CIRCUIT TECHNIQUES FOR POWER EFFICIENT ENERGY HARVESTING RECTIFIERS

BY

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This thesis is dedicated to my parents and teachers.

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All praise is due to ALLAH and peace be upon the Prophet ﷺ and his family, his companions (may ALLAH be pleased with them) and his followers.

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LIST OF ABBREVIATIONS

AC	:	Alternating Current
BANs	:	Body Area Networks
CMOS	:	Complementary Metal Oxide Semiconductor
DC	:	Direct Current
EM	:	Elecromagnetic
HF	:	High Frequency
ISM	:	Industrial, Scientific and Medical
NMOS	:	N-type Metal Oxide Semiconductor
PCE	:	Power Conversion Efficiency
PE	:	Piezo Electric
PMOS	:	P-type Metal Oxide Semiconductor
RF	:	Radio Frequency
TCD	:	Threshold Compensated Diode
UHF	:	Ultra High Frequency
WSN	:	Wireless Sensor Nodes

ABSTRACT

Full Name : Umais Tayyab

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An area of research that has garnered a lot of attention is the area of Rectifier Circuits in Energy Harvesting Systems. Energy harvesting systems eliminate wasteful batteries and long power line cables. They keep systems running without inconvenient, disruptive service calls. Energy harvesting system contains mainly a sensor, a rectifier, and a boost converter. Using a boost dc – dc converter with the rectifier gives large DC output voltage but would consume some power leading to less power conversion efficiency (PCE). Therefore, developing a rectifier circuit that produces a larger dc output voltage than its input signal amplitude would element the need for the boost converter and hence automatically improves the PCE of the system. Consequently, improving the overall efficiency of the entire system would mainly depend on the rectifier circuit's PCE.

This research is focused on the design of fully integrated energy harvesting rectifier circuit capable of providing improved efficiency and low power consumption while not compromising as much as possible on the other desirable characteristics of energy harvesting system such input sensitivity. This work proposes to merge passive rectifier (threshold forward voltage of diode is reduced and enhanced in reverse bias) and active rectifier (zero forward diode voltage drop) to form a hybrid rectifier to take the advantage of double harvested DC output voltage level and high efficiency for low power applications like biomedical implants and wireless sensor nodes. The designed circuit simulation is

carried out in Cadence virtuoso using a standard LF 0.15µm CMOS process. PCE reliance on the operating frequency, transistor sizing and output loading was assessed. The proposed hybrid configuration has achieved PCE of 79.12% at 13.56 MHz, 0.88V amplitude and 20KΩ of output load.

The thesis is arranged as follows. Chapter 1 gives the introduction while Chapter 2 provides some of the necessary background for rectifiers and some of the passive and active rectifier stage topologies in the literature. Chapter 3 discusses passive rectifier stage. Chapter 4 describes the active stage rectifier with single supply op amp. Simulation results obtained using LF 0.15µm process technology in Cadence are provided in Chapter 5. Post Layout Simulation results are given in Chapter 6. The last chapter presents the conclusion and the future work.

ملخص الرسالة

الاسم الكامل: أوميس طيب

عنوان الرسالة: تقنيات الدوائر للمقوم الكفء في نظام حصاد طاقة

التخصص: الهندسة الكهربائية

تاريخ الدرجة العلمية: 19-رجب-1438 هجري

من أهم مجالات البحوث التي تحظى بالكثير من الاهتمام هو مجال الدوائر المقومة (الموحدة) للموجات في نظم حصاد الطاقة. إن أنظمة حصاد الطاقة تتفادى إهدار البطاريات محدودة العمر وتلغي الحاجة الى كابلات خطوط الطاقة الطويلة. أنها تحافظ على عمل الأنظمة من دون توقف وتلغي الحاجة الى خدمة التصليح المتكررة. يحتوي نظام حصاد الطاقة عادةً على جهاز استشعار، الدوائر المقومة (الموحدة) للموجات، ومحول معزز للجهد الثابت. وينتج المحول المعزز للجهد الثابت جهد كهربائي أكبر ولكنه يستهلك جزئاً من الطاقة مما يقلل من كفاءة تحويل الطاقة. لذلك، فإن تطوير دوائر مقومة القادرة على انتاج جهد مباشر أكبر من سعة إشارة المدخلات من شأنه أن يلغي الحاجة إلى المحول المعزز وبالتالي يحسن تلقائيا كفاءة تحويل الطاقة. وبالتالي، فإن تحسين الكفاءة الكلية للنظام بأكمله تعتمد أساسا على كفاءة الدائرة المقومة.

ويركز هذا البحث على تصميم دائرة مقومة لنظام حصاد طاقة متكاملة قادرة على توفير كفاءة محسنة وانخفاض استهلاك الطاقة مع عدم المساس قدر الإمكان على الخصائص الأخرى المرغوبة من نظام حصاد الطاقة مثل حساسية المدخلات. ويقترح هذا العمل دمج مقوم سلبي (يتم تخفيض الجهد الأمامي من الصمام الثنائي وتعزيزها في التحيز العكسي) ومقوم نشط (الصمام الثنائي ذو الجهد الأمامي الانخفاض) لتشكيل مقوم هجين يستفيد من مضاعفة حصادها للجهد الكهربائي والكفاءة العالية لاستخدامها في تطبيقات الطاقة المنخفضة مثل الانظمة الطبية الحيوية المزروعة وعقد الاستشعار اللاسلكية. ولقد تم إجراء محاكاة الدوائر المصممة باستخدام برنامج "كيدنس فيرتيزو" وتكنولوجيا 150 نانومتر لشبه موصل أكسيد الفلز المكمِّل " سيمُس ".ولقد تم تقييم علاقة كفاءة تحويل الطاقة لدائرة المقوم المقترحة لمختلف الترددات واحجا م الترانزستور اختلاف الاحمال. وقد حقق لدائرة المقوم المقترحة كفاءة تحويل الطاقة بنسبة

79.12٪ لموجات ذات تردد 13.56 ميجاهرتز وسعة 0.88 فولت الى حمل بمقدار 20 كيلواوم. ولقد تم ترتيب الأطروحة على النحو التالي. الفصل 1 يختص بالمقدمة بينما الفصل 2 يوفر بعض من الخلفية اللازمة للمقومات السلبية والنشطة المتوفرة. ويناقش الفصل 3 مرحلة المقوم السلبي. ويصف الفصل 4 مقوم المرحلة النشط الذي يستخدم مضخم الجهد ذا مولد جهد احادي. ويتم عرض نتائج المحاكاة التي تم الحصول في الفصل 5 وكذلك نتائج المحاكاة للشريحة الإلكترونية المطبوعة في الفصل 6. ويعرض الفصل الأخير الاستنتاجات والعمل المستقبلي.

CHAPTER 1

INTRODUCTION

An area of research that has garnered a lot of attention is the area of Rectifier Circuits in Energy Harvesting Systems. As CMOS technologies have scaled down, and more functionality has been packed into integrated circuits so has the demand for efficient power management and Rectifier Circuits in Energy Harvesting Systems.

Cutting edge electronic frameworks tackle such a variety of troublesome issues however they all have the same essential restriction; they require a wellspring of electrical force. This is a test for the electronic designer as there are several power-source solutions. Off and on again a device has no immediate force source, and running wires or supplanting batteries is unrealistic. Even when long-life batteries are usable, they eventually need to be substituted.

1.1 Why Energy Harvesting?

The efficiency of devices have been expanded by advanced technical developments in capturing little amount of energy from environment and changing it into electrical form. Furthermore, progress in electronic technology have enhanced the efficiency of power and minimized the energy consumption. These improvements have started enthusiasm for engineering group to establish more applications that uses energy harvesting for power.

Energy harvesting is an increasingly tempting option for expensive batteries and inconvenient wall plugs from environment energy source where a portable application is employed. This free energy source is accessible without any support when installed properly for the whole lifetime of application. Likewise, energy harvesting is utilized as an optional energy source to supplement a primary power source and to upgrade the reliability of the overall harvesting system and avoid power interferences.

1.2 Motivation

Energy harvesting is a promptly developing zone in scientific and engineering areas because of the requirement for discovering answers to the energy issues in the world. Which power source to gather and how to do this is still noticeable all around and proper solution is reasonably application oriented. Dismissal of batteries is highly valuable for some applications such as Wireless Sensor Nodes (WSN) and embedded medical devices, where substitution of a battery is expensive or impractical. Energy scavenging offers a feasible answer for those applications.

Modern energy harvesting is utilized as it wipes out the requirement to run costly power cables to remote areas or the requirement to substitute costly primary batteries frequently. Energy harvesting systems eliminate wasteful batteries and long power line cables. They keep systems running without inconvenient, disruptive service calls.

Energy Harvesting is playing an increasingly essential role in transferring power to mobile and implanted devices. It is the procedure of seizing small amount of energy from one or all the more actually-occurring energy sources, gathering them and putting away them for future use. Energy scavenging is an increasingly tempting option for expensive and limited

life batteries and inconvenient wall plugs from a natural source where a remote application is employed, because such natural energy source is basically inexhaustible [1]-[2].

The applications of Energy Harvesting Systems can be well explained from Figure 1.

Figure 1.1 Energy Harvesting Applications

i. It is conceivable to utilize energy from the surroundings to power a self-sufficient sensorized framework such as deploying Energy Harvesting sensors to monitor remote or underwater locations.

ii. Medical embedded devices committed detecting, treatment objects are generally utilized to screen and track focused biological activities.

iii. Different forms of implantable devices are also utilized for improving the treatment and detecting efficiency by electrical incitement. Energy Harvesting provides adequate energy for backing their operations.

1.3 Energy Harvesting Systems

An Energy Harvester has typically three main blocks. It consists of power source, a rectifier for transforming environment energy into electrical from, the dc – dc voltage converter for enhancing the DC voltage and the load.

Maximum energy will be transferred to load when all components of Energy Harvester dissipates less power. Among these various components of energy harvesting, design of the rectifier circuit is crucial as it dominates the overall efficiency [1]. Therefore, this work is focusing on the design of such rectifiers. New design of energy harvesting rectifier circuits capable of providing improved characteristics are expected to evolve from this project. The proposed designs will be optimized to accomplish high efficiency and low power consumption for low power applications like biomedical devices and wireless sensor nodes.

1.3.1 Energy Harvesting Rectifier

A Rectifier is an electrical device utilized to change the generated AC signal form the transducer to DC so that it can be captured to storing device or can be used directly by the intended device. Conventional Rectifier uses diodes having forward voltage drop of 0.7V. Thus a large voltage across diode is not endured, in this way MOS diodes or even discrete Schottky diodes are prevented as transducer produces low output power and voltage.

CMOS integrated Rectifiers are separated into two parts as shown in Figure 2.

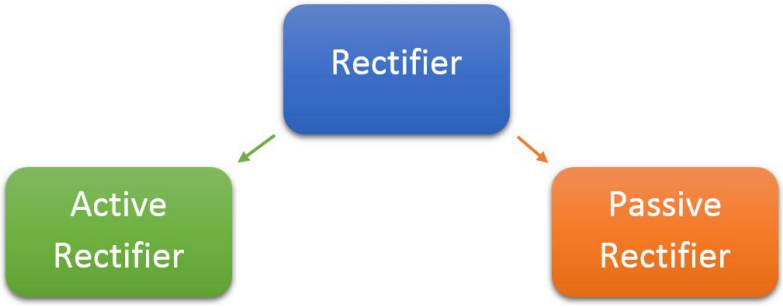

Figure 1.2 Types of Rectifier

Simple diode based rectifiers are generally prevented in CMOS due to these reasons:

i. Simple diodes are not suitable for MHz frequency range due to low switching speed.
ii. High Latch up risk
iii. Weak Characterization in the forward direction

Therefore, diode connected MOS transistors are normally utilized. The pn-junction diode voltage drop is affiliated to the V_{th} of the MOS transistor used. Basic Full wave bridge rectifier is not desirable for low voltage amplitudes due to twice V_{Th}. So, in order to enhance the PCE of the rectifier, improved circuits need to be designed to reduce the V_{Th}. Power Efficiency of passive rectifiers are less than that of Active rectifiers particularly at small incoming input signal the remaining voltage drop minimizes the performance yet the point of preference is that they fit for higher input frequencies.

Many active rectifiers have been proposed in the literature that behaves like perfect diode significance there is no forward voltage drop and no current flow in reverse direction. Despite the fact that these two properties can almost be achieved by every single active rectifier, one vast contrast exists regarding the perpetual power consumption of the control circuitry. Active rectifiers are also known as synchronous rectifiers.

CMOS integrated active rectifiers can provide higher efficiencies by generating output voltages almost at input voltage level. These features can almost be achieved by active rectifiers at the expense of power consumption.

1.3.2 Simplest Rectifier

The simplest of energy harvesting rectifier circuit is realized with a voltage doubler rectifier accepting an AC voltage as input and provides a doubled DC voltage at output. The voltage doubler rectifier will be explained later in Literature Survey Section. The switching elements are traditionally diodes driven merely by the alternating voltage of the input to switch state. However, a DC-to-DC voltage doubler does not switch in this way and hence must adopt a controlling circuit to derive the switching. They usually incorporate a switching element that can be controlled independently, such as a transistor, rather than relying on the voltage across the switch as in the diode case. Voltage doublers are a kind of single stage voltage multiplier circuit. Often, identical sections of voltage doublers are utilized in cascade to produce greater output voltage [3].

1.4 Research Objective

The aim of this research is to design energy harvesting rectifier circuit capable of providing improved characteristics in Cadence Virtuoso Simulator. The proposed research will be carried out in direction to fulfil the following objectives:

i. Investigate the possible solutions for optimizing Energy Harvesting Rectifier Circuits according to intended applications.
ii. Identifying the limits and potentials of the available solutions

iii. Modification in the rectifier design to get enhanced efficiency from low input voltage at high frequency.

iv. The basic idea is to merge passive and active rectifier stages to get better design performance and efficiency.

v. The proposed design will be optimized to reach high efficiency and less power consumption for low power applications like biomedical devices and wireless sensor nodes.

1.5 Research Methodology

The research work is divided into following tasks:

Task 1: Available solutions assessment and literature survey

i. Studying the characteristics of the different available rectifiers and evaluating their performances in order to identify the best rectifier topology.

ii. Surveying application of different techniques to design integrated energy harvesting rectifier.

Task 2: Technical Design Phase

i. The controlling factors such as input amplitude, input frequency and output loading conditions are considered.

ii. Specifications mainly type of signal provided by the previous stage, parasitic capacitance, input capacitance, input resistance and sensitivity of the next stage regulator circuit are considered.

Task 3: Rectifier Optimization Phase

- The design part will lead to main design parameters namely: Transistor sizes, Capacitor values and number of rectifier stages.
- Various Trade-offs are considered between design parameters and PCE of rectifier.

Task 4: Designing and Simulation

- The circuit design and simulations will be carried out in Cadence® and the output results will be shown.

1.6 Thesis Contribution

As of late a great deal of readings concentrated on energy harvesting systems which are utilized to scavenge typically lost natural energy and to change it into electrical energy. This result can be smart where batteries are a bottleneck for the entire system (i.e. they have a limited life time and their substitution or recharge is not possible). An energy harvesting system is an endless energy source. Energy harvesting systems can replace batteries on account of the two driving forces: power consumption reduction of the supplied electronic system and the harvesting system optimization. This latter point can be further partitioned into the energy transducer optimization and the electronic interface optimization which has to manage and store the scavenged energy.

The proposed energy harvesting rectifier circuits will be significant contributions in this important field of technology from the Kingdom. The project is applied and its results can be used for various applications, including wireless sensor distributed networks to power a

self-sufficient sensorized framework, embedded biomedical applications like wearable/implantable body area networks (BANs) for treatment and low power mobile applications.

1.7 Thesis Breakdown

The thesis is arranged as follows. Chapter 2 provides some of the necessary background for rectifiers and some of the passive and active rectifier stage topologies in the literature. Chapter 3 discusses passive rectifier stage. Chapter 4 describes the active stage rectifier with single supply op amp. Simulation results obtained using LF 0.15µm process technology in Cadence are provided in Chapter 5. Post Layout Simulation results are shown in Chapter 6. The last chapter presents the conclusion and the future work. with post layout simulations in the last chapter.

CHAPTER 2

LITERATURE REVIEW

Energy harvesting is defined as the transformation of ambient energy into electrical energy. It can also be defined as

"The collection and storage of ambient energy for on-demand, off-grid use"

The definition takes a wider, application view, where the transducer is one part of an entire system which provides power for those niche applications where other sources of energy are not available.

The three terms in the definition can be explained as follows:

i. ***Ambient Energy***: Energy is all around us, in many different forms – vibration, solar, electrical, mechanical and more. To make use of energy scavenging one or more of these energy fields must be present in the environment of interest, and there must be a suitable transducer to convert the energy.

ii. ***Off - Grid Energy***: Energy harvesting is used where another supply of energy is not available. Harvesters cost money, so it only makes sense to use them when it is too costly or physically impossible to use other energy sources such as batteries or grid electricity.

iii. ***On Demand Energy***: An energy harvester has to supply power when it is required, not simply when it is accessible, and some form of energy storage is generally required to match the demand with the supply.

This section discusses energy harvesting components and a short review on different rectifier circuit designs from the published literatures.

2.1 Energy Harvester Components

An Energy Harvester has typically three main blocks as presented in Figure 2.1.

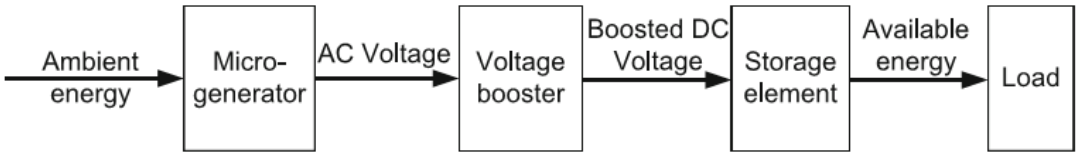

Figure 2.1 Energy Harvesting System Block Diagram

It includes ambient energy source, a micro-generator for transforming environment energy into electrical from, the voltage booster for pumping the created voltage and the storage element.

2.1.1 Energy Harvesting Generators

The choice of the energy source at last relies upon its application. Energy can be harvested from various power sources as shown in Figure 2.2.

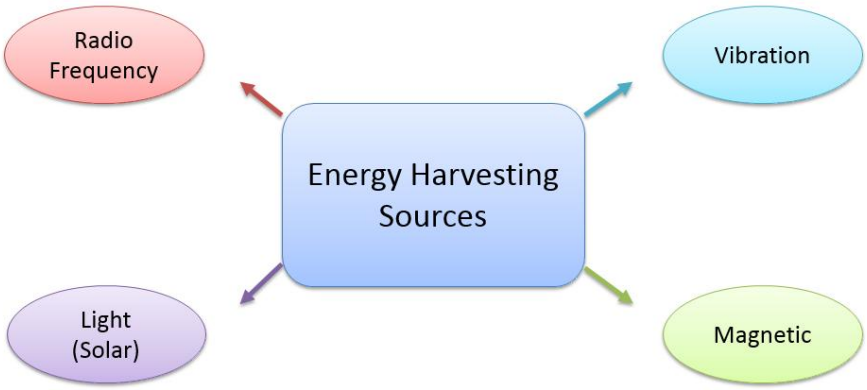

Figure 2.2 Common Sources of Energy Harvesting System Block

The accessible energy harvesting systems are separated into these fundamental parts as indicated by physical kind of energy accessible [4]:

i. **Vibration**: A large portion of the vibration energy scavenger portrayed in writing utilizes electromagnetic, piezoelectric (PE) and electrostatic, hybrid based transformation techniques. PE bimorph generators can specifically change over a forced vibration giving a generally high output voltage giving just low currents. Frequency tunable scavengers are fit for varying their resonant frequency by varying their viable beam solidness

ii. **Thermal Energy**: Thermal energy harvesting can be partitioned into thermo mechanic heat engine and thermoelectric generators. Miniaturized scale heat engines change the temperature angle into fleeting by mechanical oscillation. Thermoelectric generators exclusively compromise of Bi_2Te_3 based materials. The lifetime of thermoelectric generators increases if the weak material is not subject to solid mechanical powers.

iii. **Radio Signals**: Energy scavenging can be done from RF signals. These RF signals have specific Industrial, Scientific and Medical (ISM) radio frequency bands for certain applications such as mobile, RFID applications and the like.

2.1.2 Voltage Boosters/Multipliers

Voltage boosters are outer circuits to the small scale generator that are utilized to help up the yield voltage and to perform fundamental AC–DC correction. There are various circuit configurations that can be utilized as a voltage booster. A voltage multiplier is a particular rectifier that utilizes cascaded diodes and capacitors to accomplish higher output DC voltage from an AC input. There are two sorts of voltage multiplier taking into account diverse arrangements, to be specific Villard and Dickson [5].

2.1.3 Storage Element

Capacitor is usually employed as storage element in Energy Harvesting System. A super capacitor has been modelled in case of Wind Energy Harvesting [6]. RF Energy Harvesting System is employed in charging a battery (storage element) [7].

2.2 Why Rectifier?

The boost converter circuit usually contains an Inductor. Inductor is not successful in Integrated Circuits because it is difficult to fabricate. It physical structure is that of a coil. All elements in integrated circuits are horizontal not vertical and fabrication is done with rectangular/square size. Now, multilayer/simulated inductors are made but they are more expensive.

The conventional dc – dc converters are Inductive type dc – dc converters that are appropriate for medium-to-heavy load range only [8]. Switched Capacitor dc – dc converters [9] require a clock signal. Although it achieves high linearity but the addition of dc – dc converter with the rectifier gives large area in the integrated circuit design. So, in energy harvesting system there is an additional device (converter) with rectifier that means more power consumption (less efficiency). The DC power can be directly scavenged if the rectifier's output voltage is more than the energy storage component [8]. The energy harvesting circuit with boost converter in [10] is used for high power devices.

2.2.1 Rectifier's PCE

Maximization of the PCE of the whole system mainly relies on the performance of rectifier circuit. In fact, enhancement in the PCE of the rectifier is considered as a distinctive and powerful way to upgrade the efficiency of the entire system. This is because the performance of front-end are often limited by regional regulations. For example, the maximum power transmission allowed in the Japan and U.S is 4 W while the allowable antenna area is 1.64 for the dipole antenna [11]. The PCE of rectifier circuit is described as ratio of the output power to the input power. The input power equals to the loss in the rectifier plus the output power. Thus, PCE can be expressed as:

$$PCE = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT}+P_{LOSS}} \tag{2.1}$$

When current flows through the diode there occurs resistive loss which is called diode loss. It is the sum of the forward and reverse losses of the diode. These are usually calculated from the diode forward voltage drop and the diode reverse leakage current [11].

2.3 Rectifier Circuits

Operation of conventional rectifying circuits assumes relatively high voltage input (few volts). In such application, however, the available voltage for rectification falls underneath 0.3 V in radio frequency (RF) to DC rectification system, much too low to defeat the traditional rectifier circuit's threshold voltage. The Schottky diode with turn-on voltage of 0.2–0.3V might have been employed but this component requires additional processing cost and is not accessible in a standard CMOS process. The following subsection presents a very attractive rectifier design for this application known as voltage doubler rectifier. Subsequently, several approaches for improving the PCE of voltage doubler rectifier through circumventing or diminishing the "dead-zone" in voltage rectification are presented. The main solutions are classified as static V_{th} cancelations methods including a very important solution known as self-driven synchronous rectifier, floating gate topology and active V_{th} cancellation methods.

2.3.1 Voltage Doubler Rectifier

For the scheme of the RF-DC power rectification systems, voltage doubler rectifier structure is typically utilized as it produces output DC proportional to double of the approaching radio frequency signal amplitude and can be organized in cascade to enhance the DC output voltage [12]. The voltage doubler rectifier also called charge pump circuit is demonstrated in Figure 2.3. It comprises of a voltage clamp shaped by D_2 and C_1 and peak rectifier framed by D_1 and C_2.

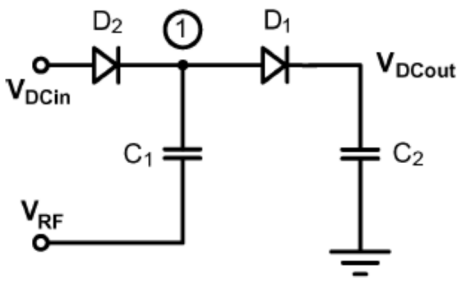

Figure 2.3 Diode Based Voltage Doubler Rectifier [12]

For the one stage rectifier, V_{DCin} is zero but for multistage rectifier it would be the DC output of the preceding stages. It can be shown that the DC output voltage of the circuit is:

$$V_{out} = 2|V_{RF}| - V_{DO1} - V_{DO2} \tag{2.2}$$

where $|V_{RF}|$ is the amplitude of input RF signal. Clearly, in addition to its primary rectification role, this circuit has the advantage of acting as voltage-multiplier (doubler) increasing the produced DC voltage level. Minimizing cost is a primary goal for many power extraction applications, and hence, standard CMOS processes are preferred. The corresponding MOSFET based voltage doubler rectifier is shown in Figure 2.4.

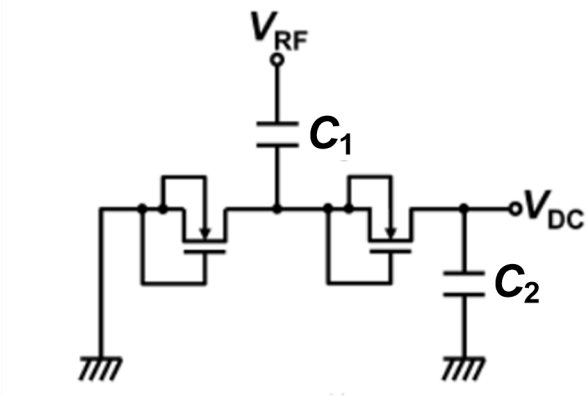

Figure 2.4 MOSFET based Voltage Doubler Rectifier [11]

The second point of preference of the voltage doubler rectifier is that it can be connected in cascade to further enhance the generated DC voltage level. An N-stage voltage multiplier approximately provides N-times larger dc output voltage than its counterpart of a single stage. An N-stage voltage multiplier comprises of a cascade of peak-to-peak detectors, as can be seen in Figure 2.5 [13].

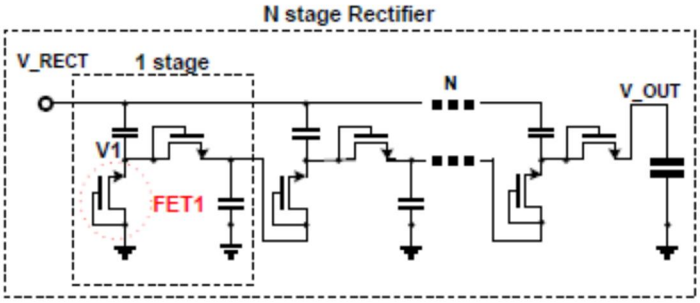

Figure 2.5 CMOS Voltage Multiplier [13]

The diode-connected MOSFET transistor's effective turn-on voltage and the MOSFET transistor's threshold voltage are almost equal. It is bigger than its Schottky diode counterparts not as much as its pn-junction diode. Thus, the diode-connected MOSFETs rectifiers have limited PCE.

2.3.2 Static V_{th} cancellation methods

Several Vth cancellation schemes were suggested in [14], [15], and [16] for reducing the effective turn-on voltage and hence leading to better PCEs. The threshold voltage minimization technique presented in [14] needs the incoming voltage to be relatively extensive to start the circuit. The second drawback of this solution is that the produced bias voltage is considerably less than the sought threshold voltage. The switched-capacitor technique presented in [15] and [16] uses an external power supply for generating the

required DC gate bias voltage. Besides, they require extra circuitry to generate differential clock which itself necessitate a secondary battery. Also, they suffer from the same constraint i.e. generating relatively low bias voltages for diode-tied transistors. In general, switched-capacitor has a fundamental limitation on their operation of switches when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages.

The self-V_{th}-cancellation rectifier generates gate bias DC voltage from the rectifier's output voltage itself among other static V_{th} cancellation methods [11] and [17]-[19]. This is achieved by connecting the NMOS transistor to the output node and the PMOS transistor's gate electrode to ground as shown in Figure 2.6. Indeed such approaches achieve small diode loss. However, they suffer from loss of reverse leakage which enhances for bigger gate bias voltage.

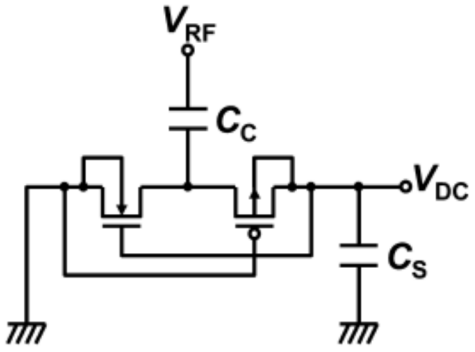

Figure 2.6 Self V_{th} Cancellation Scheme [11]

2.3.3 Floating Gate Solution

Floating gate solution presented in [12] does not require extra circuitry and hence avoids both the need for a secondary battery and redundant power consumption that would be consumed by the biasing circuit. The rectifier circuit's threshold voltage can be

programmed by utilizing floating-gate rectifier scheme. The entire circuit structure is alike as that of a voltage doubler rectifier of Figure 2.3 for the floating-gate rectifier configuration. The diodes are supplanted by diode connected floating gate transistors as shown in Figure 2.7.

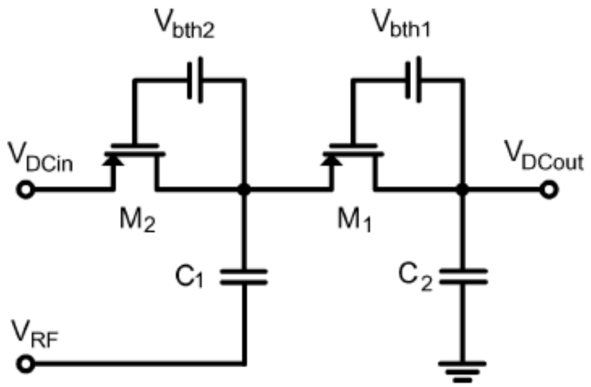

Figure 2.7 Voltage Doubler Rectifier employing PMOS floating gate [12]

PMOS floating gate implementation formed by a MOS capacitance and a normal transistor is shown in Figure 2.8. The MOSFET transistor's threshold voltage is lessened through infusing few charges on its gate. This is usually achieved when a high voltage is applied to the gate causing the electrons be caught in the oxide because of the tunneling effect [12].

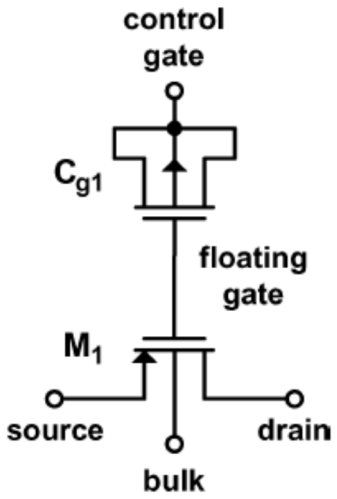

Figure 2.8 Implementation of PMOS floating gate [12]

However, this method is not practical as the alteration is needed for every single transistor utilized in the diode-tied arrangement. Also, after some time the captured charges are discharged steadily, hence the threshold voltage goes to the initial state. This means that this technique is bad for long-haul operation particularly for the new small size CMOS process having extremely small oxide thickness [20].

2.3.4 Special Transistor Solutions

Another solution is by utilizing zero-threshold transistors for voltage rectifier. However, these devices have zero threshold only for a range of minor current. The threshold voltage V_{th} of the transistors can be lessened in few processes giving native gadgets [20].

2.3.5 Self-Driven Rectifier

Static V_{th} cancellation schemes achieve a small ON-resistance but suffer from large reverse-leakage current. The works in [11], [21], and [22] suggest a solution to this problem. In this method V_{th} is reduced in forward bias configuration and raised in reverse

bias configuration consequently by a cross-coupled differential rectifier setup. Figure 2.9 demonstrates the single phase differential-drive CMOS rectifier circuit.

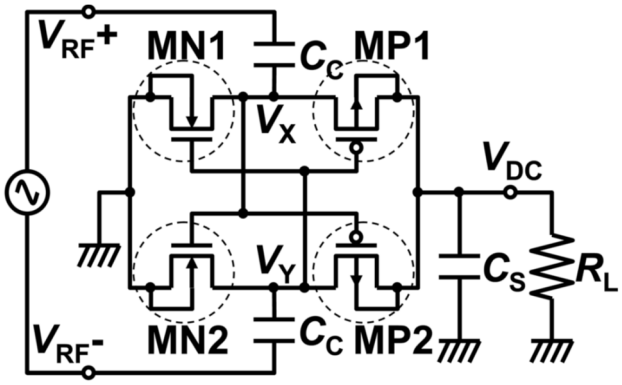

Figure 2.9 Differential drive CMOS rectifier circuit [11]

The rectifier has a bridge structure with a cross-coupled differential CMOS setup. The operation of the circuit will be described in the next chapter. It reduces the forward voltage drop and reverse leakage current hence enhancing the PCE of the rectifier. This solution assumes the availability of differential input signals. Also, it may not be connected in cascade to generate higher output voltage. Another self-driven rectifier was referred to as a threshold compensated diode (TCD) in [23]. TCDs were used to build voltage doubler cell. Four of these cells were utilized to realize voltage multiplier using multistage rectifier based on Dickson topology. The main drawback is that its implementation requires the use of large capacitors (80pF) which were off chip. Also, the achieved PCE of 37.8% is relatively low.

2.3.6 Active V_{th} cancellation methods

The efficiency of energy harvesting circuit can be improved by using active rectifier (zero forward diode voltage drop). This is achieved through increasing the harvested DC voltage level via the use of some active elements. It is expected that the power gained due the

increased output DC level is more than the power loss of the adopted active elements. For example,

i. The design in [24] uses two stage active rectifier having first stage of CMOS transistors and second stage of PMOS transistors and one comparator. One specialized issue is the offset of comparators for comparator-based active-diodes because of process variations that causes oscillation and leakage to consequence in enhanced energy loss. Active-diodes based on op-amp can lighten the issue [25].

ii. An active full-bridge rectifier adopting operational amplifier-based active diode and a switch in parallel with the transducer is presented in [25]. The supply voltage of op-amp comes from the harvested energy. The proposed solution uses two opamps to implement full-bridge rectifier. Also, it assumes input signal with low frequency 200Hz.

iii. More recently, a reconfigurable rectifier using two modular rectifier blocks was presented in [7]. The two rectifiers can be combined either in parallel or in series through the MOSFET switches controlled by the control logic signal. According to the available RF power, this signal is generated by the control logic circuit. But the logic sub circuit assumes the availability of DC voltage supply. They were after improving the efficiency and sensitivity. The reported sensitivity is -21dBm, however, the achieved efficiency is only 60%.

2.4 Benchmark Table

Table 1 summaries the main characteristics of the available designs in the literature and highlights their drawbacks.

Table 2.1 Summary of the available Solutions

Available Solution	Main characteristics	Drawbacks
[11], [12], [13]	Voltage Doubler Rectifier with Diode-connected MOS transistor	-Turn-on voltage drop loss may not be used for low input harvesting systems.
[15],[16]	Static V_{th} cancelations using switch capacitor technique	-Extra circuitry to generate differential clock. -Generate relatively low bias voltages. -Problem with low voltage operation. - Suffer from gate leakage problems. -Associated with switching noise.
[11] and [17]-[19]	Self-V_{th}-Cancellation scheme	- Suffer from reverse leakage loss.
[12], [20]	Voltage doubler rectifier employing PMOS Floating gate	- Not cost effective requiring special set ups. - Not reliable as threshold voltage returns to its initial state gradually. - Not good for long-term operation for new small size CMOS process having small oxide thickness
[11], [21], and [22]	Differential Self-driven rectifier	- Require differential input voltages. - It may not be connected in cascade to generate higher output voltage.
[23]	Threshold compensated diode (TCD) based rectifier	- Requires large capacitors 80pF (off chip) - Low PCE of 37.8%.
[24]	CMOS Comparator based scheme	- The offset of comparators causes oscillation and leakage to result in increased power loss. - Assume input signal with low frequency 100Hz. - Assume C_L=10μF
[25]	Op-amp-based active-diodes	- Use of two op-amps to implement full-bridge rectifier. - Assume input signal with low frequency 200Hz. - Assume C_L=1μF
[7]	Active-V_{th}-cancelation of the self-driven rectifier	- Require voltage supply for the controlling circuit. - Improve PCE to only 60%.

2.5 Research Project Design

Energy Harvesting System primarily consists of a micro generator sensor, a rectifier, a voltage booster and a storage element/load. The energy harvesting circuits with boost converters are used for high power devices. As harvesting systems are typically intended for low power applications, voltage boosters may be avoided in most applications. The research project design is decomposed into two parts, Circuit Level specifications and System Level specifications. All the parameters are investigated in circuit and system level to optimize the energy harvesting rectifier and to improve the power conversion efficiency.

2.5.1 Circuit level Design

As it can be seen from the literature survey of recent publications, new energy harvesting rectifier circuits improves the power efficiency but has some disadvantages like leakage problem in comparator, additional bias circuitry required for op amp and TCD based rectifier. These constraints needs to be further resolved to enhance the efficiency of energy harvesting system according to the required applications.

The PCE and output power are the most significant factors for systems continuously operating off harvested power. These are influenced by rectifier topology, transistor-device parameters, input amplitude and frequency, and output load as demonstrated in Table 2.2. These factors are carefully studied to achieve the optimum results.

Table 2.2 Performance of the Available Solutions

Reference	[11]	[12]	[23]	[24]	[25]	[7]
Technology (um)	0.18	0.25	0.35	0.35	0.18	0.13
Topology	Differential Self-driven rectifier	Voltage doubler rectifier employing PMOS Floating gate (36 stages)	TCD with 5 stages	Active Rectifier (Comparator)	Op-amp based active diode	Reconfigurable Differential CMOS rectifier with cross connected transistor scheme
Input	-12.5dBm (75mV) (C_S=1.13pF)	-22.6dBm – (5.5uW) (23.4mV)	0.5V	0.5V	2.8V	-21dBm (28mV)
Input Frequency	953MHz	906MHz	13.56MHz	100Hz	200Hz	868MHz
Output	Not available	Not available	2.5V	Not available	2.78V	2V
Area	0.78 mm × 0.78 mm	400 um × 1000 um	Not available	0.38 mm × 0.19 mm	0.4 mm × 0.6 mm	0.4 mm × 0.5 mm
PCE	67.5% (R_L=10kΩ)	60% (R_L=0.33MΩ)	37.8% (R_L=180kΩ)	90% (R_L=50kΩ)	90% (R_L=95kΩ)	60%
Output Power	Not available	Not available	35.8uW R_L= 180kΩ C_L= 80pF	25uW R_L=50kΩ C_L=10uF	81uW R_L=95kΩ C_L=1uF	Not available
DC Power Consumption	Not available	Not available	Not available	(266 nW)	90nA	Not available

It can been form Table 2.2 that the passive rectifier solutions such as [11], [12] and [23] can process high frequency input signals which is the typical case of harvesting systems.

But they achieve relatively low PCE in the range of 37.8% to 67.5%. On the other hand, the active rectifier such as [24] and [25] assume low input frequency and relatively large dc input (minimum 0.5V) but achieve PCE of approximately 90%. The reconfigurable rectifier of [7] showed an improved sensitivity but failed to improve the efficiency (efficiency of 60% was reported).

2.5.2 System level Design

At system level, we concentrate on selected rectifier type and investigate its performance under system level constraints related to the incoming radio frequency signal amplitude and frequency, and the loading conditions at the output. For example, the issue of adoption of rectifier incorporating transistors that operates in the sub-threshold region. This is expected to allow processing of extremely small power but its implementation depends on how the cutoff frequency of the transistors in sub threshold compared with the input RF signal frequency.

Trade-offs between transistor sizes and the rectifier performance are studied. It is observed that smaller transistors has less parasitic capacitance but small transistors gives low current to the load and hence lowering the rectification efficiency. Also, reducing a channel width increase the ON-resistance of the diode-tied transistors.

Multi-stage rectifiers are studied to achieve the optimum design performance. The number of stages should provide sufficient output voltage to operate regulator. Yet, the utilization of an excess of stages of rectifier damps out the impact of the high-resonator.

CHAPTER 3

RECTIFIER DESIGN: PASSIVE STAGE

This chapter begins with major idea of the proposed rectifier design for incoming RF signal. The first stage of the rectifier is discussed in this chapter. The simulation is carried out in Cadence® with 0.15um CMOS technology and results will be displayed. PCE of the rectifier depends on the RF input frequency, output load and transistor sizing values and it will be evaluated in this chapter. The multistage configuration is also demonstrated for larger DC output voltage.

3.1 Passive Rectifier Stage

Regarding the passive rectifier stage, it has been found that the self-driven synchronous rectifier performs better than diode-based rectifiers [11]. Also, differential self-driven CMOS rectifier results in the most attractive solution as it achieves less ON-resistance and less reverse-leakage current simultaneously. In this method V_{th} is minimized in a forward bias condition and increased in a reverse bias condition automatically by a cross-coupled differential circuit configuration but it would need differential RF signals. The input differential signal problem can be remedy through the use of differential antenna such that reported in [7].

3.1.1 RF Energy Harvesting

Energy harvesting from radio frequency (RF) has been around for decades, yet only recently have designers begun to unravel its vastly untapped potential: a limitless power

source. Broadcasting RF energy to power remote devices is suitable for RF identification (RFID), biomedical and wireless sensor networks (WSN) applications. In addition, it provides momentous advantages over battery-powered solutions (e.g., low operational and assembly costs), amid negligible environmental effects. RF energy harvesting system has the least power density when compared to other power sources like light, vibration etc.

RFID applications are hastily increasing in the fields of logistics, access control, supply chain management and the like [26] – [28]. A basic RFID tag is passive (no battery). RF signals are radiated from the reader that are used to power RFID. So, the RF power transmission limits the communication range. RFIDs are usually known in terms of radio frequency (RF). There are ISM bands reserved for RF energy to be utilized internationally for industrial scientific and medical purposes (applications). Telecommunication is excluded from ISM bands. The ISM bands are provided by ITU radio regulations and frequency is allocated for different license users. When RFIDS are to be used for long term communication to transfer power/data, Ultra High Frequency band (860 – 960MHz) or other high frequency bands are considered that uses far field electromagnetic (EM) wave transmission. The High Frequency (HF) band (3 – 30MHz) utilizes near field EM wave transmission with less communication distance (less than 1m). A Highly Efficient Active Rectifier is presented in [29] operating at 6.78MHz for portable charger and biomedical devices. The rectifier in RFID chip is operated at 6.78MHz for low power dissipation transmission through the tissue of human body and the communication frequency is 866MHz [30]. A full-wave active rectifier operating at 13.56 MHz for a wide input range for wirelessly powered high-current biomedical implants is presented in [31]. Therefore, Harvesting the EM power wirelessly emitted in the Industrial, Scientific and Medical (ISM)

band (6.78, 13.553–13.567, 300–348, 387–464 and 779–928 MHz bands) is an alluring alternative for remote power devices among available energy sources [32].

3.1.2 RF PCE

Power originating from RF energy sources may be unregulated, alternating and/or small. Therefore, in such situations it becomes dominant to enhance the PCE of the rectifier. The HF RFID communication range can be extended if the PCE of the rectifier is improved/enhanced. As the output of the rectifier can be the input of the next stage or to power an active element, so larger PCE is desired so that next stage give more DC output voltage with feasible efficiency for its proper operation. If the PCE of the first stage is bad then 2nd stage is useless to be utilized for further operation.

The threshold voltage (V_{th}) of passive diodes and diode-connected MOS transistors confines the maximum PCE of a charge-pump rectifier [33], thereby confining the maximum power delivered to the load. The diode connected MOS transistors generally has worse PCE than Schotkky diode but V_{th} cancellation technique has better PCE as discussed in Chapter 2.

The PCE of the rectifier is defined in chapter 2, equation (2.1). To further enhance the definition, P_{Loss} is defined as

$$P_{LOSS} = N.P_{DIODE} \tag{3.1}$$

P_{DIODE} is the loss in the diode and N is the total number of diode stages [34,35].

When current flows through the diode, the resistive loss generated the diode loss and is expressed as:

$$P_{DIODE} = P_{FWD} + P_{REV} \tag{3.2}$$

P_{FWD} is the diode forward drop and P_{REV} is the diode reverse drop. These two are found by the diode voltage turn on and the diode leakage reverse current.

An active cross-coupled differential rectifier circuit setup is presented in [11] at RF signal frequency of 953MHz. In this method V_{th} is reduced in forward bias configuration and raised in reverse bias configuration consequently. The center frequency of 13.56MHz (allocated in ISM band for mobile and fixed users) is employed in this passive stage of the rectifier for HF RFID.

3.2 Differential Drive CMOS Rectifier

Figure 2.9 demonstrates the single phase of the differential-drive CMOS rectifier circuit [11] which can be also shown here in Figure 3.1.

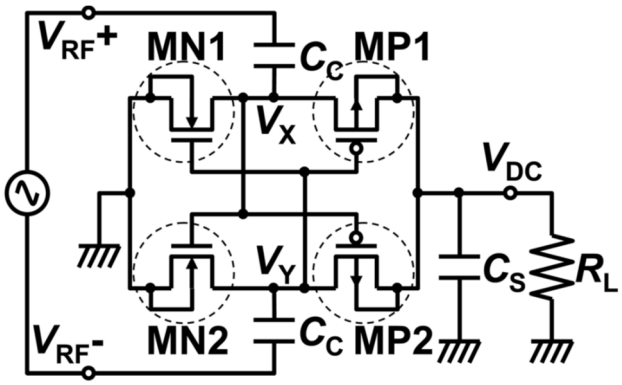

Figure 3.1 Differential drive CMOS rectifier circuit [11]

The circuit has a bridge structure with a differential CMOS cross-coupled setup. The rectifier utilizes input differential configuration and could be easily attached to an antenna like dipole antenna.

The operation of the rectifier circuit is described as follows. The common-mode voltage equal to the DC segments of V_X and V_Y is about one half of the DC output steady-state voltage. It is generated as on the other static V_{th} cancellation schemes by a rectification process and goes about as static bias gate voltage compensating V_{th}. This would lead to output DC voltage of,

$$V_{out} = 2|V_{RF}| - V_{drop} \tag{3.3}$$

where V_{drop} represents losses due to switch on resistance. On the other hand, differential-mode signal actively biases the gate of transistors. When V_X is negative during forward biasing of MN1, MN1's (V_Y) gate voltage is biased positively and hence minimizes MN1's turn on voltage. This outcomes in little turn on losses. Whereas when V_X is positive (during the reverse bias operation), the gate voltage quickly minimizes and hence decreases the turn off losses.

The input power sensitivity of the rectifier is -12.5dBm. The antenna receives minimum power (-12.5dBm) from the RF signal. This power cannot drive the rectifier circuitry as input voltage amplitude should be greater than the V_{th} of the CMOS transistor. So, an impedance matching circuit is employed between antenna and the rectifier to get input voltage more than the V_{th} of the CMOS transistor.

3.2.1 Voltage Waveforms

Figure 3.2 depicts the voltage waveforms of the internal nodes. DC voltage of 0.62V is generated under the steady state condition when the input is 0.88V. This DC voltage acts as static gate bias voltage to compensate V_{th}. The differential mode signal makes the gate of the transistor actively biased.

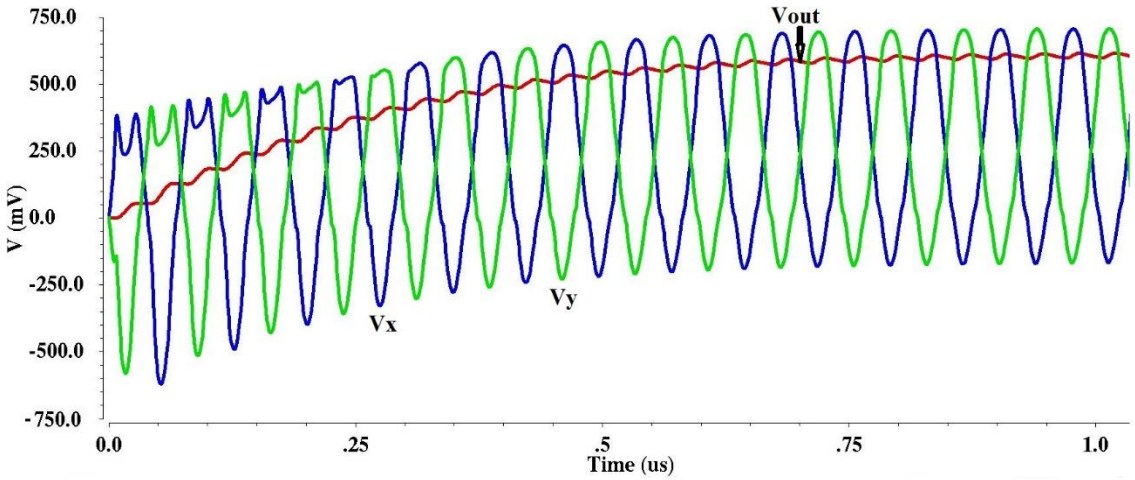

Figure 3.2 Voltage waveforms of internal nodes

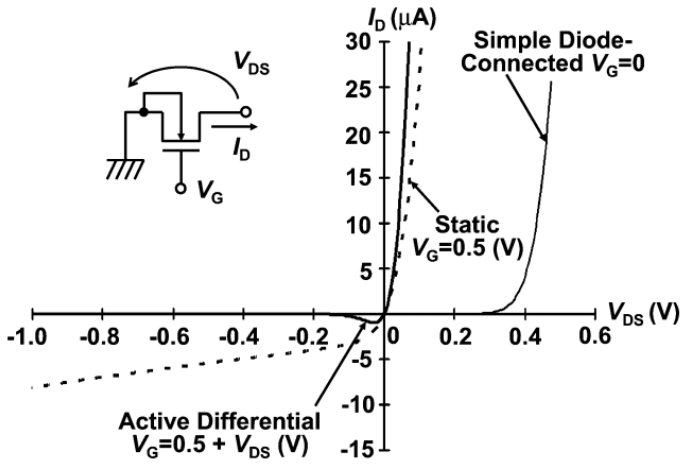

Figure 3.3 I-V characteristic of diode transistor (NMOS)

Figure 3.3 demonstrates simulated diode NMOS transistor I–V characteristics. W/L of the NMOS transistor are 3 μm/0.18 μm. The static V_{th} cancellation and active differential V_{th} cancellation configurations are evaluated in figure 3.3. As an example, gate bias DC voltage for both circuits are set to 0.5V. Static gate bias voltage reduces ON-resistance for static V_{th} cancellation case in contrast with the simple diode-connected configuration, but also enhances the leakage reverse current leading to diode loss and reduction in the PCE. Leakage reverse current is immediately prevented by a negative gate bias in the active

differential V_{th} cancellation scheme. Therefore, both lower ON-resistance and lower leakage reverse current are concurrently achieved.

3.3 Results and Discussions

The simulation results are presented here is carried by using Cadence Virtuoso Simulator with 0.15µm CMOS process technology. Channel Width/Length of NMOS transistor is 3µm/0.18µm and channel Width/Length of PMOS transistor is 18µm/0.18µm for optimized results. The threshold voltage (V_{th}) of the NMOS is 0.5V and that of the PMOS is -0.56V. The center frequency of 13.56MHz (allocated in ISM band for mobile and fixed users) is employed. The values of coupling capacitor and load capacitor is set to 40pF.

3.3.1 PCE dependence on Input Signal

The PCE dependence on Input signal of Differnetial drive circuit is simulated and is compared with Self V_{th} cancellation scheme [10-11]. It is shown in Figure 3.4.

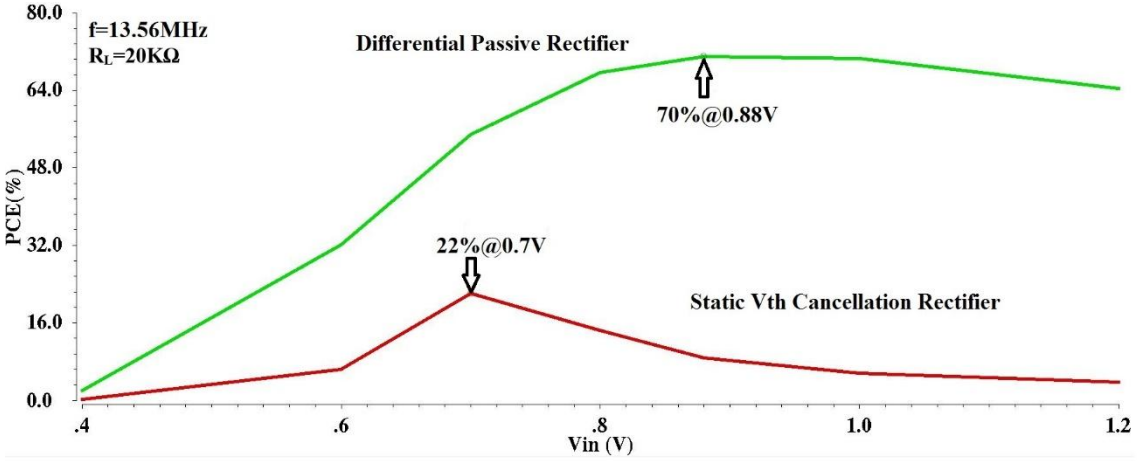

Figure 3.4 PCE as a function of V_{in}

PCE as a function of input voltage is plotted in Figure 3.4. The simulation is carried out at frequency of 13.56MHz and load resistance of 20KΩ. The differential drive rectifier achieves 70% at input voltage of 0.88V and is the highest PCE ever reported at 13.56MHz from incoming RF signals. The PCE of self V_{th} cancellation scheme is 8.76% at 0.88V which is 8.3 times less than the differential CMOS Rectifier.

PCE decreases as the input voltage goes beyond 0.88V similar to the Self V_{th} cancellation scheme. When the static bias gate voltage for CMOS transistor becomes huge then the leakage reverse current of the CMOS transistors enhances under bigger input voltage condition.

Figure 3.5 shows DC output voltage versus input voltage when compared to Self V_{th} cancellation scheme.

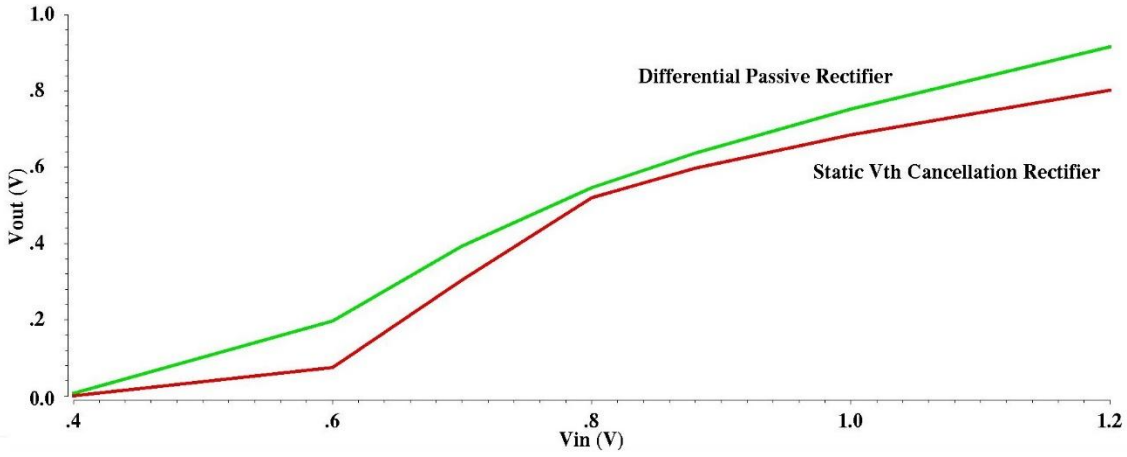

Figure 3.5 DC output voltage as a function of V_{in}

It can be seen DC output voltage rises with increase in input voltage and it is clear that DC output voltage of differential rectifier is greater than Self V_{th} cancellation scheme rectifier.

3.3.2 PCE dependence on Input frequency and load

PCE of the rectifier depends upon its operation frequency. Figure 3.6 shows the frequency dependence on PCE of the rectifier verses the input voltage.

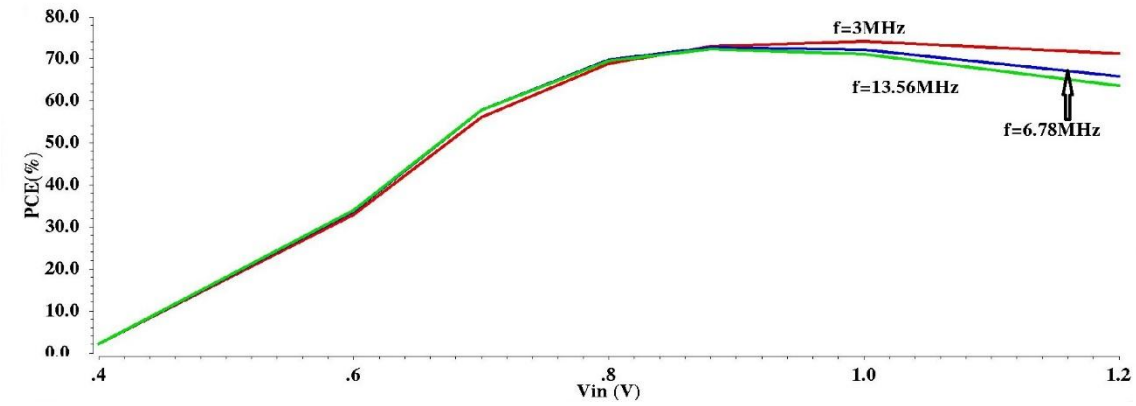

Figure 3.6 Frequency dependence of PCE

PCE remains almost same (minute difference in PCE for high frequency) for low input voltage but after its peak value, PCE decreases with increase in frequency. This is due to the parasitic resistance that causes energy loss enhances from the rise in the high frequency current rolling in the rectifier because of rise in the input reactance.

When the load resistor increases, PCE of the rectifier increases for the lower input signal as shown in Figure 3.7. It is also shifted towards left side (towards low input voltages). This means that the larger PCE can be obtained at low inputs when the load resistor is large. PCE of 79% is obtained at 0.7V input when load resistor is 100KΩ. This means that communication or wireless power transmission (biomedical application) can be done at such low input with high PCE.

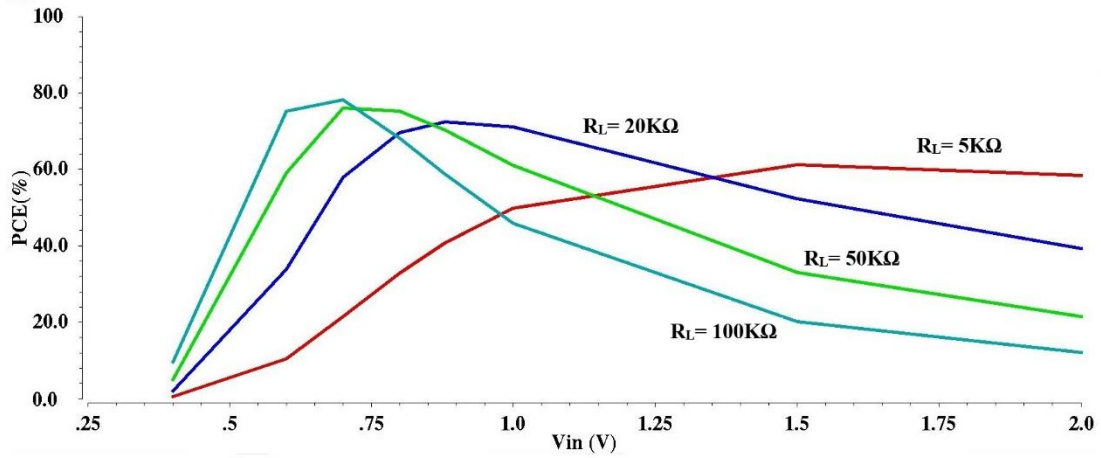

Figure 3.7 Load Resistor dependence of PCE

The PCE of the rectifier depends upon the output loading condition and its simulation is demonstrated in Figure 3.8. Input amplitude is 0.88V. The highest PCE is 70% at R_L= 20KΩ. The PCE decreases with the load resistor due to the phenomenon of maximum power transfer. When the rectifier input impedance equals the output impedance, maximum power is transferred to the load which leads to the large efficiency of the circuit.

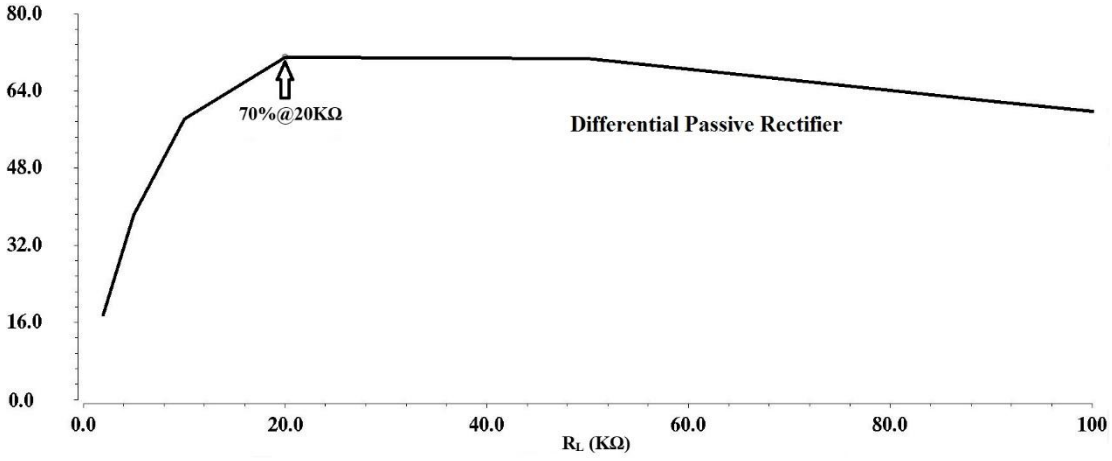

Figure 3.8 PCE as a function of R_L

3.3.3 PCE dependence on Transistor sizing

The rectifier transistor ratios affects the performance in PCE which is clearly visible in Figure 3.9

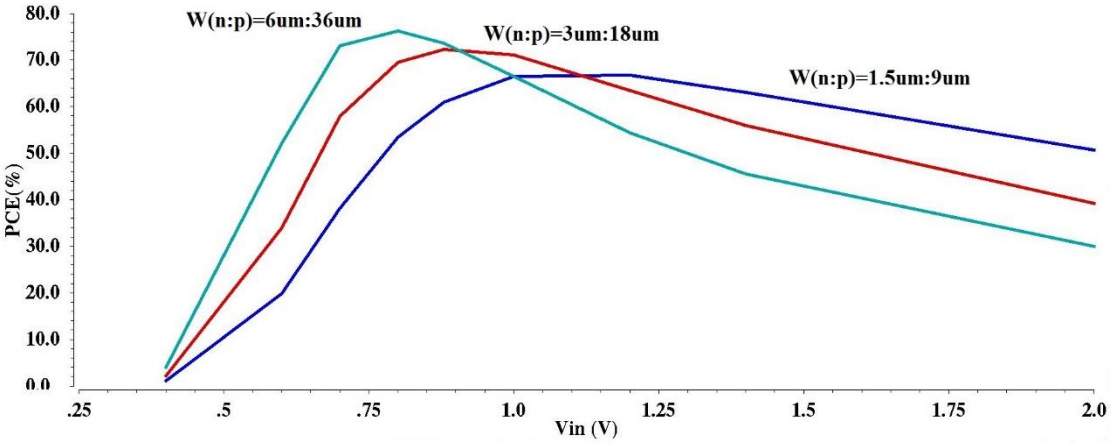

Figure 3.9 PCE as a function of transistor sizing

The transistor width sizes are 3µm (NMOS) and 18µm (PMOS) while length of these transistors are same 0.18µm. The width sizes of transistor are designed to be narrowed (half) and wider (double) while maintaining the width ratio of NMOS and PMOS same i.e 6 for balanced function of rectifier.

At input signal of 0.8V the wider transistor has more PCE than the narrower ones at R_L=20KΩ and it achieves larger peak PCE of 76.2%. This is because the wider transistor have small ON resistor than the narrower ones at this load. At higher inputs, narrower transistors have more PCE than the wider transistors as it has less leakage reverse current than the wider transistors.

3.4 Multistage Differential Rectifier

The output DC voltage is obtained several input differential rectifier circuit as can be seen in Figure 3.5. The output voltage form 0 to 1V is obtained for different variations in the PCE that can be seen in Figure 3.4. Sometimes this DC voltage is not sufficient for biomedical implant circuit and digital baseband circuits in RFID, they require larger voltage for its proper operation i.e. more than the input signal. For larger output voltage multistage configuration can be used as shown in Figure 3.10

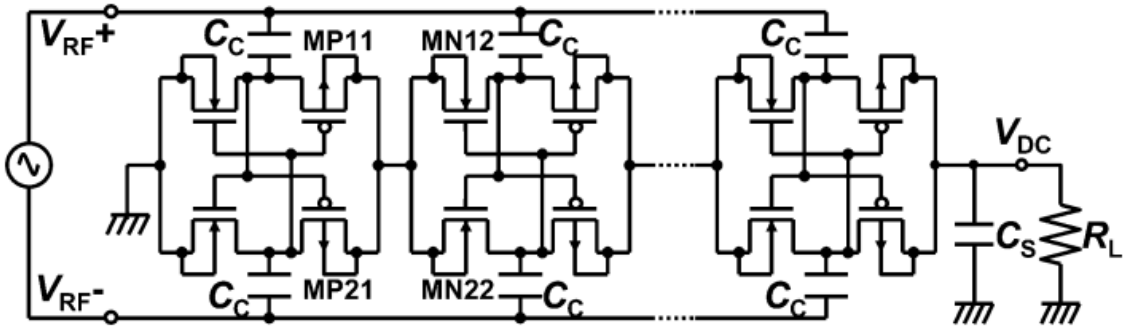

Figure 3.10 Multistage Rectifier [11]

The stages are serially cascaded along the DC path to each other and merged in parallel from the differential input signal. This scheme can be used to obtain larger DC output voltage and is operated to the point where larger PCE can be achieved. The output capacitor of first stage which is now the inner stage capacitor can be of small value or can be removed. If the NMOS and PMOS between the two stages are well matched, smaller value of capacitance can minimize the ripple. The two stage rectifier is simulated and the output DC voltage and PCE is plotted to understand its operation. These results are compared with single stage rectifier.

Figure 3.11 shows the output DC voltages of single stage and double stage as function of input voltage. For smaller inputs the output voltages for both the schemes are same but it increases as the input voltage increases.

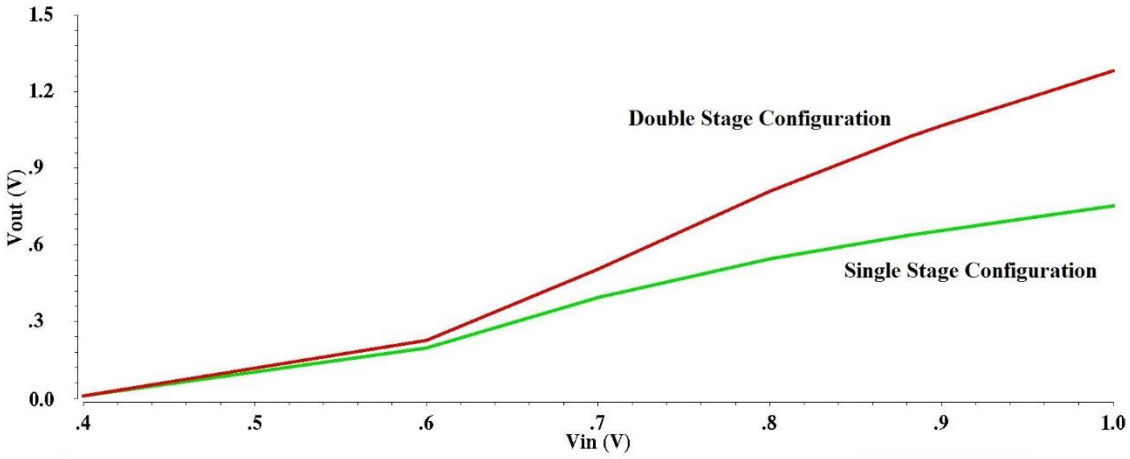

Figure 3.11 Output voltage vs Input voltage (Single and Double Stage compared)

PCE becomes slightly smaller than the single-stage rectifier at low input signals In the multi-stage scheme. The stages are merged in parallel to the input signal as mentioned earlier and it supresses the rectifier's input impedance in the multi-stage configuration. Thus, the voltage amplitude of the multi-stage scheme becomes slightly smaller (almost same) than the single-stage rectifier and this results in the reduction in PCE as adequate input voltage amplitude greater than the V_{th} of CMOS transistor is necessory for attaining larger PCE. For example, when the input voltage is 1V, adequate output DC voltage of 1.23V is obtained while maintaing 64.24% of PCE when compared to single stage rectifier.

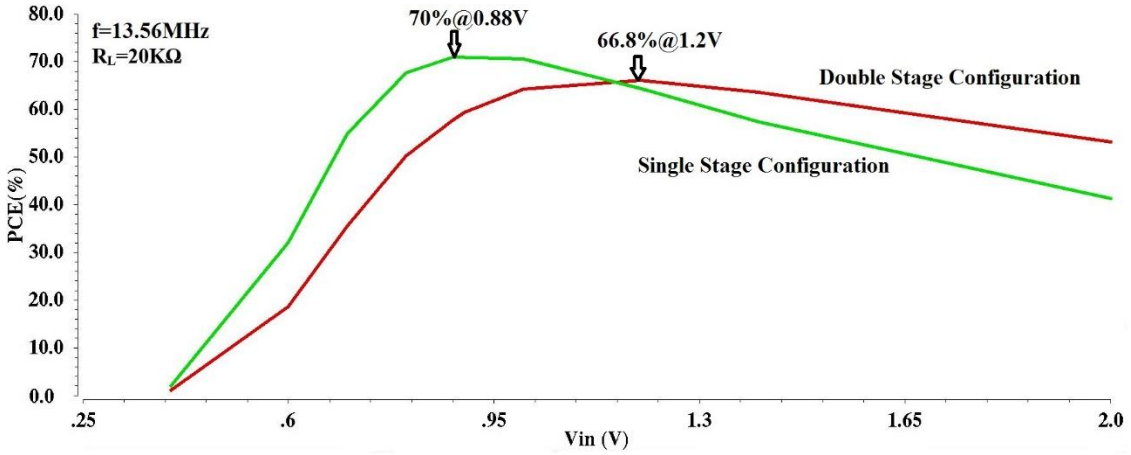

Figure 3.12 PCE vs Input voltage (Single and Double Stage compared)

3.5 Conclusion

A high-efficiency CMOS rectifier circuit for HF RFID and biomedical implants applications with an active V_{th} cancellation configuration is designed [11]. The rectifier reduces the V_{th} of CMOS transistors in a forward bias and enhance it in a reverse bias by a cross-coupled circuit scheme. The circuit has a PCE of 70% at 13.56 MHz, 0.88V of input amplitude and 20 KΩ of output loading. The PCE of self V_{th} cancellation scheme is 8.76% at 0.88V which is 8.3 times less than the differential CMOS Rectifier. The multi-stage scheme was assessed as to be effective in order to realize bigger DC output voltage without reducing PCE.

CHAPTER 4

RECTIFIER DESIGN: ACTIVE STAGE

This chapter begins with idea of the active rectifier for incoming RF signal at VHF band. Large PCE in the rectifier can be achieved by the use of an active element i.e. Op Amp. The simulation of active element is carried out in Cadence® with 0.15um CMOS technology and results will be displayed. Power consumption dependence of op-amp on the unity gain frequency will be evaluated in this chapter.

4.1 Active Rectifier Stage

For the active rectifier stage, comparator based topology will be avoided in order to element power loss due to oscillation [24]. The first suggestion is to adopt switched opamp technique in active rectifier designs. This work may extend the switched opamp technique applied to filters [36] to propose new rectifier designs. But it requires clock signal for switches so one has to be careful if PCE of the rectifier is main parameter in the design. The other suggestion is to adopt active-V_{th}-cancelation of the rectifier based on self-driven opamp design [25].

4.1.1 Vibration Energy Harvesting

Various environmental energy sources, like RF, thermal, and solar energy, can be powerful alternatives to replace or assist batteries via energy scavenging. Particularly, vibration energy, among the ambient energy sources, happens in many surroundings including buildings, cars, trains, aircraft, and ships. Piezoelectric (PE) energy scavenging systems

provide a fairly high energy density going from 10 to several hundreds μW/cm^3 [37]. Vibration energy scavenging using PE generator can provide 300 μW/cm^3 approximately in surroundings where low level vibrations happen [38]. A Rectifier is required that converts the AC output from PE transducer into DC.

4.1.2 Precision Rectifier

When op amp is used with a diode, a precision rectifier is formed [39]. The precision rectifier is also referred to as "Super Diode" as shown in Figure 4.1.

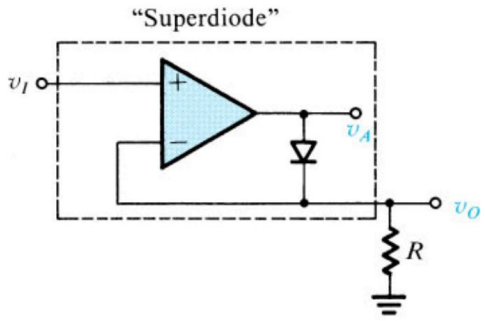

Figure 4.1 Super diode Half wave Rectifier [48]

The circuit conducts for positive input signals as the diode conducts and with the establishment of negative feedback structure the output voltage equals the input voltage. For negative inputs the output of the op amp is negative so the diode is cut off and there will be no current in the load resistor R, causing output voltage to be zero as can be seen in Figure 4.2.

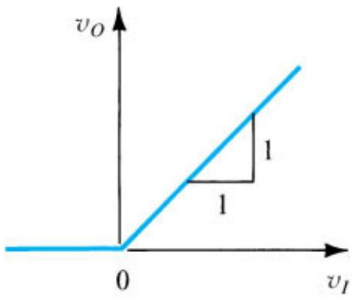

Figure 4.2 Ideal transfer characteristics of Super diode [48]

As the diode is off the feedback loop is gone. The op amp is in open loop condition and its output is negative saturation level. Therefore, the precision rectifier effectively reduces the forward V_{th} of the diode. But for negative inputs the output is in saturation level. Of course this is true if the op amp has dual supply. Actually, this is an advantage for differential rectifier circuit [11] as discussed in Chapter 3. For negative inputs, the gate MOS transistor is negatively biased to reduce the reverse leakage current. But dual supply op amp consumes more power and will degrade the PCE of the rectifier. Single supply op amp can be used to reduce the power consumption.

4.1.3 Main Limitation of Op-amp based rectifier

The main hurdle in op amp based active rectifiers is that the op amp itself requires DC power supply. There are two drawbacks if DC power supply is used for op amp:

i. Additional element and additional price has to paid every time the circuit is utilized for certain application

ii. Addition of DC supply means more power consumption which degrades the PCE performance of the active rectifier.

Above mentioned drawbacks can be eliminated if the DC supply of the op-amp based rectifier comes from the harvested energy [25], [40]. When the DC supply of the op-amp is coming from the harvested energy no need of an additional supply. It saves the price. The stored energy in the capacitor is positive voltage DC and this energy is fed back to bias the op amp. Hence, op-amp must be single ended supply as only positive DC rectified voltage is coming from the output of the proposed rectifier. Now, the only problem left is the power consumption of the op amp. If the op amp power consumption is less than the remaining circuit of the rectifier then the PCE of the active rectifier can be improved otherwise there is no use for op-amp in the rectifier design

4.2 Op-amp Design

Although the dual supply op amp is advantageous to implement, there are many applications where single supply op amp is required. For example, Computers can have a built in single supply power (+5V or +12V). In marine and automotive equipment, battery power provides single supply. One of the main advantage of single supply Op-amp is low power consumption and hence it is useful for low power applications (less power consumption) such as biomedical implants and wireless sensor nodes. But single supply op-amp need appropriate signal biasing otherwise the op-amp becomes unstable or does not provide the desired output. A single supply differential pair MOS configuration [41] is adopted as shown in Figure 4.3.

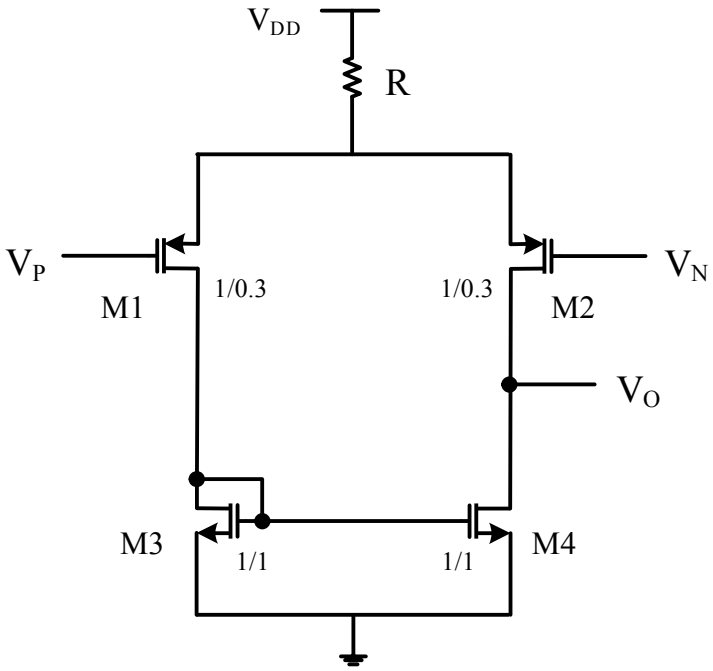

Figure 4.3 Single Supply Differential Amplifier [50]

The differential pair configuration in [41] is different than the differential pair configuration presented in [48]. The PMOS input differentials (M1 and M2)) are used which are matched. The sources of these PMOS transistors are connected together with tail current (resistor in this case) which in turn is connected to DC power supply. Consequently, the active loads are NMOS transistors (M3 and M4). All the transistors are operating in pinch off region condition and the op-amp has been carefully optimized for better performance.

4.2.1 Frequency Response of Op-amp

The op-amp is powered with 0.6V DC supply and transistor Widths and Lengths are all set to 1µm except for PMOS width, it is set at 0.3µm. The tail resistor is set to 125KΩ. The frequency response of the op amp is demonstrated in Figure 4.4.

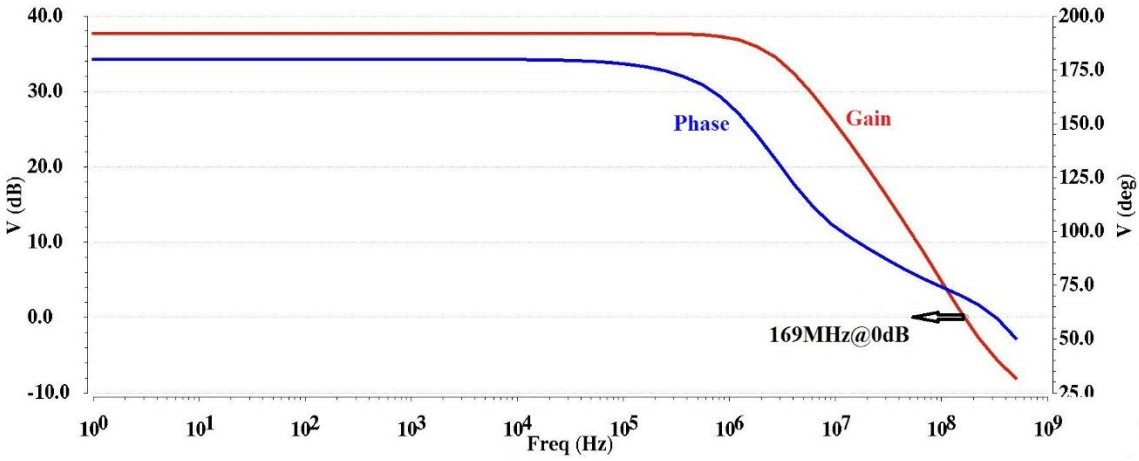

Figure 4.4 Simulated Frequency Response of Differential Amplifier [50]

The gain and phase response of the op amp is simulated and shown in Figure 4.4. The 3dB gain of the op amp is 38.05dB and the unity gain frequency is 169MHz. The tail current can be varied by varying the tail resistor or by adding a tail PMOS transistor (should in pinch off). Changing W/L of tail transistor changes the value of current. The current consumption of the op-amp is 310nA at 0.6V supply.

4.2.2 Relation between power consumption and unity gain frequency

The gain 'A' of the op-amp is given by the relation:

$$A = A_D + A_{CM} \tag{4.1}$$

A_D is the differential gain and A_{CM} is the common mode gain of the op-amp.

The frequency response of op-amp at different tail resistors (70KΩ, 125KΩ and 250KΩ) is simulated in Figure 4.5

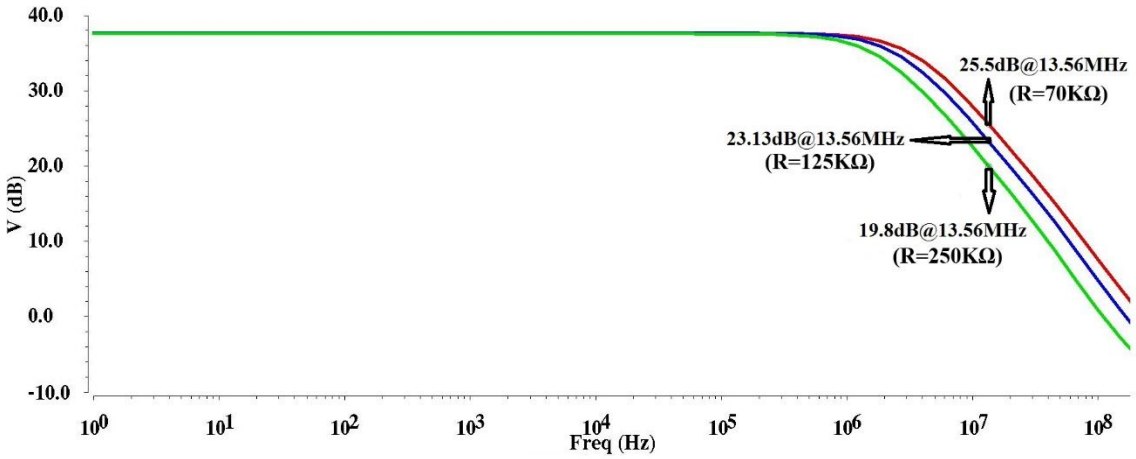

Figure 4.5 Simulated Frequency Response at 70KΩ, 125KΩ and 250KΩ

The current consumption of op-amp at tail resistors 70KΩ, 125KΩ and 250KΩ is 435nA, 310nA and 200nA. Of course current consumption in the op-amp will be more for higher supply DC values.

It can be seen from the waveforms when tail resistor is increased then less current is consumed in the op-amp and also unity gain frequency decreases for larger tail resistor. Varying the bias current varies gain of the op-amp and also the unity gain frequency as can be seen in equation 4.2. The unity gain frequency (ω_T) is given by the relation:

$$\omega_T = \frac{g_m}{C_c} \tag{4.2}$$

g_m is the gain of op-amp and C_c is the compensation capacitor. The gain increases by using small tail resistor but results in more current consumption as can be seen in Figure 4.5. Thus, here is tradeoff between current consumption and unity gain frequency.

4.3 Op-amp without DC power supply

An active self-supplied rectifier is presented in [42] in which op-amp is biased from harvested energy. The op-amp based rectifier with MOSFET switch (diode) is shown in Figure 4.6.

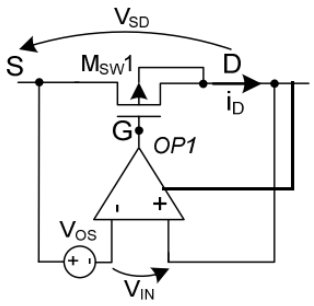

Figure 4.6 Op-amp based diode switch M_{SW1} [51]

The function of the circuit is described as follows. The source of PMOS is connected to AC input and the drain of the PMOS is connected to load capacitor and resistor. The output goes to DC supply of op amp. When the circuit starts op-amp cannot work as there is supply to op-amp from input. Instead the PMOS diode conducts as source of PMOS is connected to AC input. The DC energy stored is given to op-amp from which op-amp starts working giving larger output voltage and PCE. The circuit can be seen as lower efficiency passive one and higher efficiency active one. The passive one works during only at startup and then active stage dominates the circuit performance.

Applying Kirchhoff law in Figure 4.5

$$V_{IN} + V_{SD} - V_{OS} = 0 \tag{4.3}$$

The output voltage of op-amp is given as:

$$V_G = A.V_{IN} \tag{4.4}$$

where A is defined as DC gain of the operational amplifier.

V_G can be found by equating equation (4.3) and (4.4):

$$V_G = A.(V_{OS} - V_{SD}) \tag{4.4}$$

The difference in equation (4.4) has to diminish for finite V_G when DC gain of op-amp is considered ideal. Therefore, a regulation loop is achieved which maintains V_{SD} of the MOS transistor equal to offset voltage V_{OS} for each value of the drain current.

4.4 Conclusion

The rectifier design in [42] is for high input voltage 1.5V and low frequency 200Hz. Although the rectifier achieves high efficiency but has limitation for low inputs and high frequency (RF signals). Also no output voltage is shown in [42] only PCE performance is shown. The proposed design of the thesis is to combine the designs in [11] and [42] to achieve larger output voltage and higher efficiency from the incoming RF signal. The details of the proposed design are in the next chapter.

CHAPTER 5

PROPOSED DESIGN: HYBRID RECTIFIER

This chapter presents the proposed rectifier design for incoming RF signal at 13.56MHz operating frequency. The simulation is carried out in Cadence® with 0.15um CMOS technology and results will be displayed. PCE of the rectifier depends on the RF input frequency, output load and transistor sizing values and it will be evaluated in this chapter. The proposed rectifier is compared with the differential CMOS rectifier presented in Chapter 3. The multistage configuration is also demonstrated for applications that require larger DC output voltage and feasible PCE.

5.1 Proposed Design

This work proposes the combination of passive and active rectifier structures to form an integrated hybrid rectifier. The differential CMOS configuration in [11] is passive rectifier and op-amp based scheme in [42] is the active voltage doubler. The NMOS and PMOS transistors diodes in [42] are connected as super diode i.e. precision rectifiers. The purpose is to make the forward voltage drop zero and reverse leakage current zero in order to achieve greater efficiency. The active voltage doubler [42] achieves high efficiency of about 90% but at high input AC voltage 1.5V and relatively low frequency 200Hz. Also, the load capacitance value is 1uF so it not integrateable. The differential drive circuit [11] has RF input antenna receiving signal of -12.5dBm (f=953MHz) and is converted to 0.88V differential voltage signal by the help of impedance matching circuit [7]. This differential signal of 0.88V is fed to rectifier and maximum power conversion efficiency of 67.5% is

achieved. In order to get high PCE in the rectifier design, two things need to improve. First the forward voltage drop in the diode must be zero and second less reverse leakage loss in the diode is desired. The design in [11] is modified by using two diodes as precision rectifier [42] in order to make forward voltage drop to zero and reverse leakage current to zero. The hybrid rectifier stage (cell) can be connected in cascade to form voltage multiplier in order to increase the output DC voltage level. Since, the efficiency of first stage (passive rectifier) [11] is around 67% and its counterpart of active stages (active rectifier) [41] is 90%, the proposed hybrid solution provides power conversion efficiency of approximately 79% at 0.88V (same input level as in [11]).

5.2 Hybrid CMOS rectifier

Figure 5.1 presents the hybrid CMOS rectifier circuit with two NMOS super diodes.

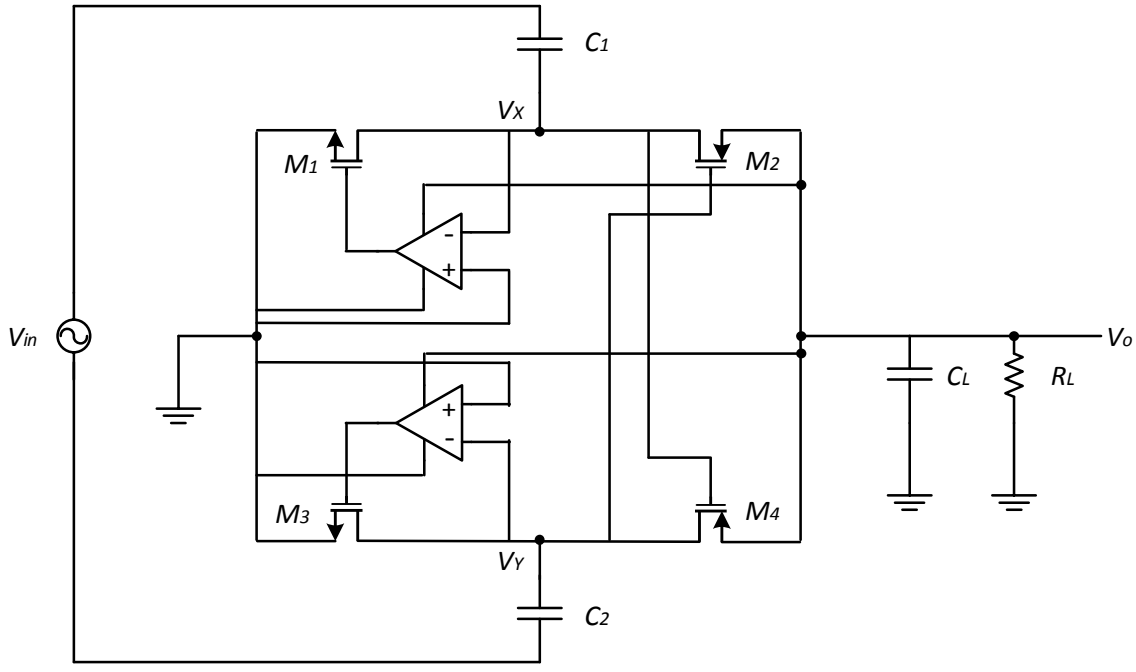

Figure 5.1 Proposed Hybrid CMOS Rectifier

The proposed hybrid rectifier demonstrated in Figure 5.1 has two op-amps connected with NMOS transistors in a precision rectifier stage and the shown configuration is optimized to give 79.12% efficiency for low input signals.

The circuit has a bridge structure with a cross-coupled differential CMOS setup with two op-amp diodes connected to NMOS transistor. The output of the op-amps are connected to gate of NMOS transistors. The positive inputs of op-amp is grounded and op-amp is biased from the output DC voltage of the hybrid rectifier meaning there is no additional DC supply. The negative inputs of the op-amps are connected to their respective input differential signal as can be seen in Figure 5.1. The hybrid rectifier also utilizes input differential configuration and can be easily merged to an antenna such as dipole antenna [11].

The hybrid rectifier is designed in the same way as Differential CMOS Rectifier [11] to make the circuit operation same. When V_x is positive PMOS (M2) will be ON (V_y is negative) and M1 will be in reverse bias condition. The negative input of op-amp is connected to V_x and positive is grounded so the output level will be negative voltage. Since the op-amp is single supply, biased from output DC voltage, the output of the op-amp will become zero (gate voltage of M1 will become zero) to make NMOS (M1) transistor off thus leading to negligible reverse leakage current. At the same time V_y is negative which makes the output of the bottom op-amp positive turning ON M3. When V_x is negative, NMOS (M1) diode is in forward bias condition, the output of the upper op-amp quickly goes to DC output voltage (gate of M1 is positively biased) and it reduces the turn ON gate voltage of M1 transistor, causing in a less ON resistance of the transistor.

The input power sensitivity of the rectifier is -12.5dBm. The antenna receives minimum power (-12.5dBm) from the RF signal. This power cannot drive the rectifier circuitry as input voltage amplitude should be greater than the V_{th} of the CMOS transistor. So, an impedance matching circuit should be employed between antenna and the rectifier to get input voltage more than the V_{th} of the CMOS transistor.

5.2.1 Voltage Waveforms

Figure 5.2 depicts the voltage waveforms of the internal nodes. DC voltage of 0.73V is generated under the steady state condition when the input is 0.88V. This DC voltage acts as static gate bias voltage to compensate V_{th}. The differential mode signal makes the gate of the transistor actively biased with two op-amps.

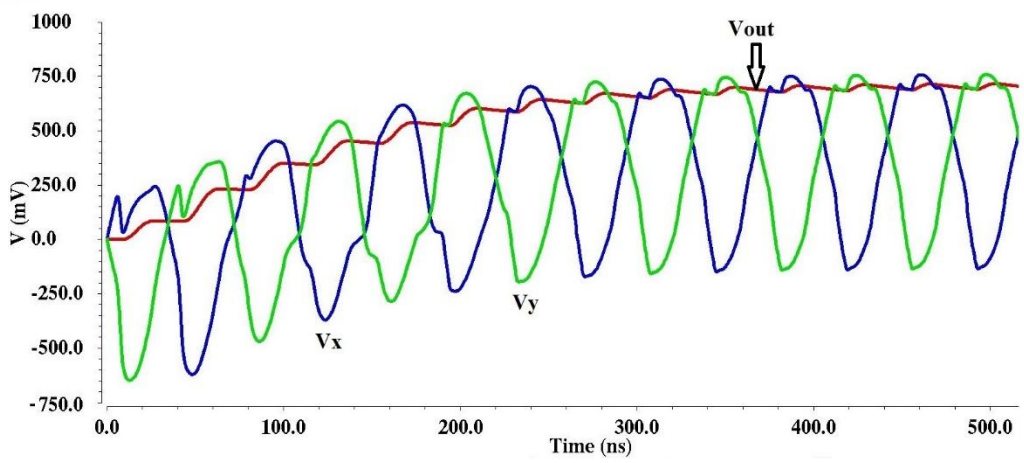

Figure 5.2 Voltage waveforms of internal nodes

5.3 Results and Discussions

The simulation results are presented here is carried by using Cadence Virtuoso Simulator with 0.15µm CMOS process technology. Channel Width/Length of NMOS transistor is 6µm/0.15µm and channel Width/Length of NMOS transistor is 18µm/0.15µm for

optimized results. The threshold voltage (V_{th}) of the NMOS is 0.5V and that of the PMOS is -0.56V. The center frequency of 13.56MHz (allocated in ISM band for mobile and fixed users) is employed. The values of coupling capacitor and load capacitor is set to 40pF.

5.3.1 PCE dependence on Input Signal and load

The PCE dependence on Input signal of Hybrid CMOS rectifier circuit is simulated and is compared with Differential drive CMOS rectifier circuit [11]. It is shown in Figure 3.4.

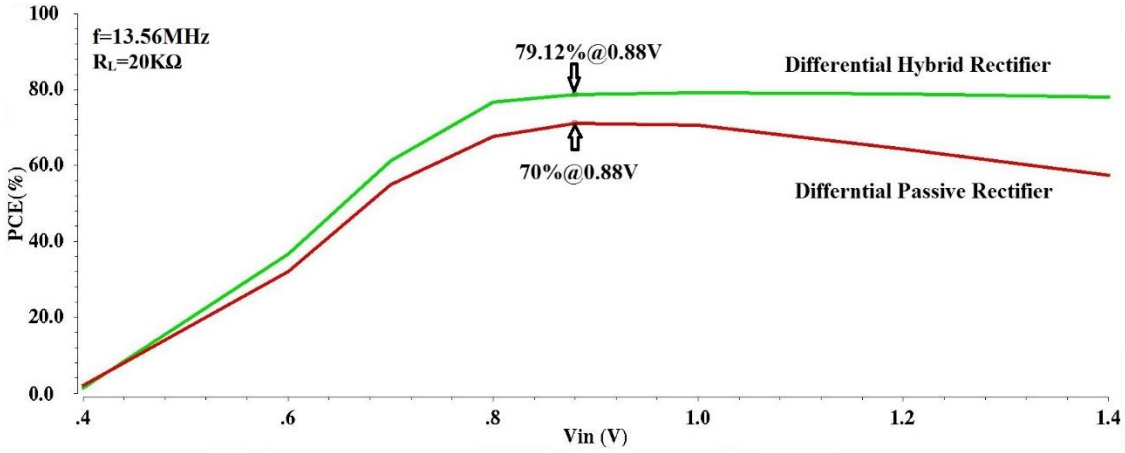

Figure 5.3 PCE as a function of V_{in}

PCE as a function of input voltage is plotted in Figure 5.3. The simulation is carried out at frequency of 13.56MHz and load resistance of 20KΩ. The differential drive rectifier achieves 79.12% at input voltage of 0.88V and is the highest PCE ever reported at 13.56MHz from incoming RF signals. The PCE of differential passive rectifier is 70% at 0.88V (same W/L ratio as of hybrid) and is 9.12% less than Differential CMOS hybrid rectifier.

PCE is low for Input signals less than 0.6V but larger than the differential passive rectifier. PCE starts to increase after 0.6V input signal but the op-amp does not starts to fully operate.

The op-amp does not function properly before 0.75V input so it cannot control the gate voltages of NMOS properly. The V_{th} of PMOS is -0.56V for 0.15µm process technology. At 0.75V the DC output voltage of hybrid rectifier becomes 0.563V and is fed to bias the op-amp, thus PMOS differential pair starts to fully conduct. Beyond 0.75V input voltage PCE increases as the op-amp starts working properly and continues to remain at 79.5% for larger inputs as can be seen in Figure 5.3. For the differential passive rectifier, when the static bias gate voltage for CMOS transistor becomes huge then the leakage reverse current of CMOS transistors enhances under bigger input voltage condition.

Figure 5.4 shows DC output voltage versus input voltage when compared to Differential passive rectifier scheme.

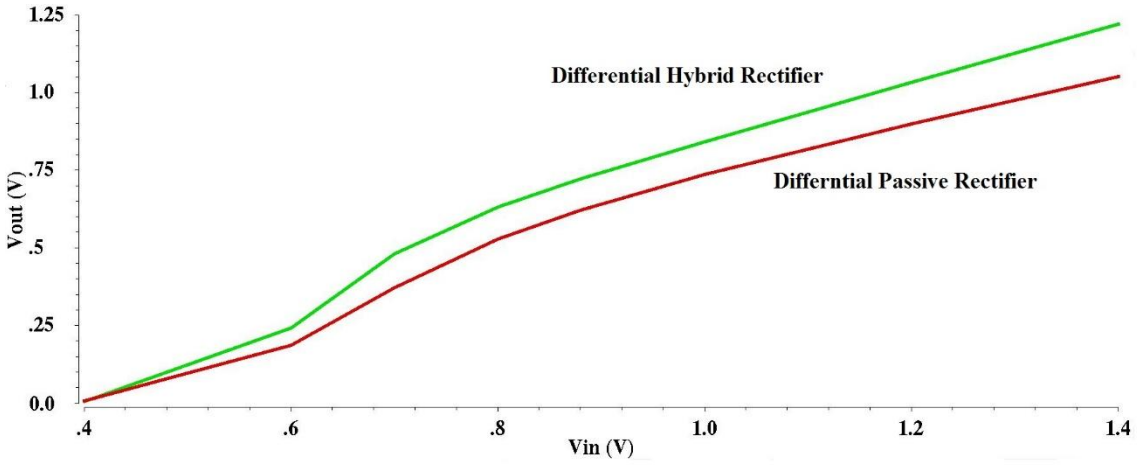

Figure 5.4 DC output voltage as a function of V_{in}

It can be seen DC output voltage rises with increase in input voltage and it is clear that DC output voltage of Differential Hybrid rectifier is greater than the differential passive rectifier scheme. The summary of Figure 5.3 and Figure 5.4 is presented in Table 5.1

Table 5.1 PCE and Output Voltage when R_L=20KΩ

Vin=0.7V	Passive Rectifier (13.56MHz)	Hybrid Rectifier (13.56MHz)
Vout (V)	0.362	0.51
PCE (%)	53.86	62.28
Vin=0.8V		
Vout (V)	0.52	0.631
PCE (%)	66.36	76.62
Vin=0.88V		
Vout (V)	0.6	0.73
PCE (%)	70	79.12
Vin=1V		
Vout (V)	0.73	0.842
PCE (%)	68.6	79.13
Vin=1.2V		
Vout	0.88	1.04
PCE (%)	64.37	79
Vin=1.4V		
Vout	1	1.22
PCE (%)	57.36	78.91

The minimum operating voltage of the hybrid rectifier is 0.6V as it gives the output voltage of 0.25V. Below 0.6V the output voltage is negligible, for example, at 0.4V differential input give 5.3mV output and when the input is above 0.7V the op-amp starts giving better efficiency.

The PCE of the rectifier depends upon the output loading condition and its simulation is demonstrated in Figure 5.5.

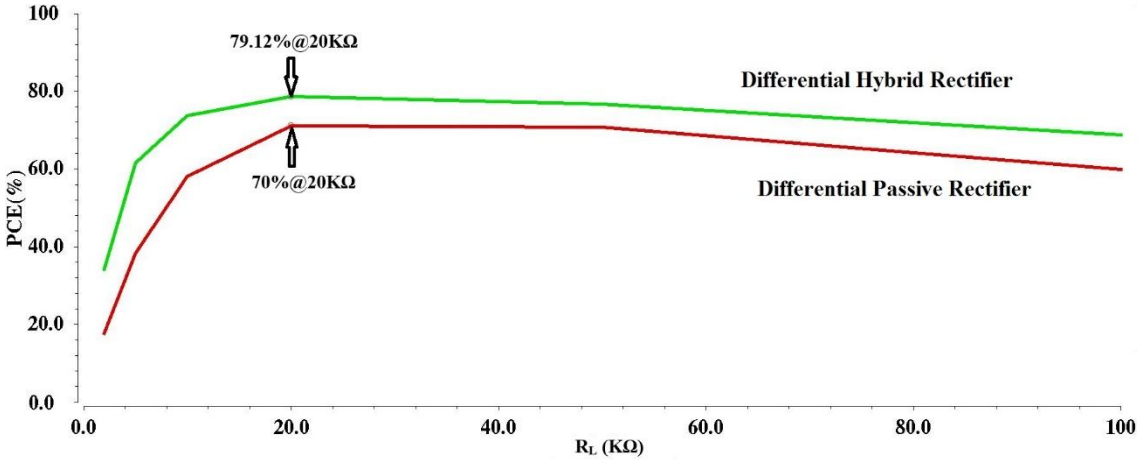

Figure 5.5 PCE as a function of R_L

The highest PCE is 79.12% at R_L= 20KΩ at input amplitude of 0.88V. The PCE decreases with the load resistor due to the phenomenon of maximum power transfer. When the rectifier input impedance equals the output impedance, maximum power is transferred to the load which leads to the high efficiency of the rectifier at that particular point. The maximum power transferred for active is high 20KΩ load than passive rectifier and even after that PCE is higher than differential passive rectifier. It is clear that Differential Hybrid rectifier is best for all loading conditions than differential passive rectifier [11]. The summary of Figure 5.5 is presented in Table 5.2

Table 5.2 PCE and Output Voltage when V_{in}=0.88V

R_L =5K	Passive Rectifier	Hybrid Rectifier
Vout (V)	0.32	0.55
PCE (%)	38.32	61.53
R_L =10K		
Vout (V)	0.49	0.65
PCE (%)	57.14	73.72
R_L =20K		
Vout (V)	0.61	0.73
PCE (%)	70	79.12
R_L =50K		
Vout (V)	0.7	0.771
PCE (%)	69.1	76.72
R_L =100K		
Vout	0.73	0.8
PCE (%)	58.83	69.77

5.3.2 PCE dependence at different loads and on Input Frequency

PCE of the rectifier depends upon its operation frequency. Figure 5.6 shows the frequency dependence on PCE of the rectifier verses the input voltage.

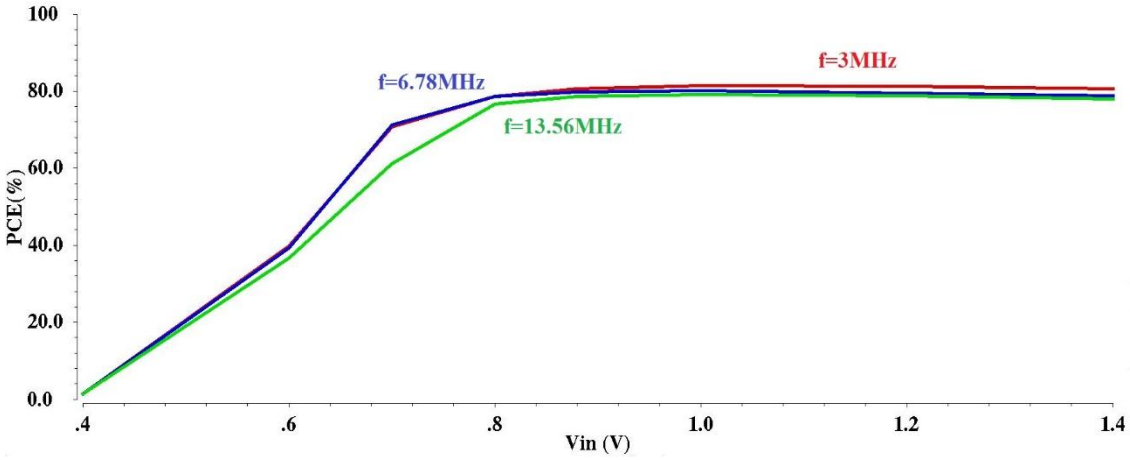

Figure 5.6 Frequency dependence on PCE

Lower frequency has better PCE dependency than the higher frequency. The PCE for 13.56MHz slightly lower than other two frequencies for almost all input voltages. To understand this we need to go back on Chapter 4 and examine the frequency response of the op-amp in Figure 4.4. Let's say at 0.6V supply voltage of op amp, the unity gain frequency is 85.67MHz. When frequency is low the gain is more and hence PCE with respect to input voltage will be more. When shifting towards high frequency gain becomes less and hence at low input voltages, PCE at 13.56MHz is slightly lesser. At high input voltages the unity gain frequency increases and shows better response at high input signals. One can select 6.78MHz for portable charges and biomedical devices [29] and for RFID chips [30] operating at 6.78MHz. The selection of frequency for Differential Hybrid Rectifier is 13.56MHz as this frequency is widely used for low power applications as RFID tags, wireless sensor nodes and the like [11], [31].

PCE decreases with increase in frequency. This is due to the parasitic resistance that causes energy loss enhances with the rise in the high frequency current passing in the hybrid rectifier because of the rise in the input reactance.

When the load resistor increases, PCE of the rectifier increases for the lower input signal as shown in Figure 5.7.

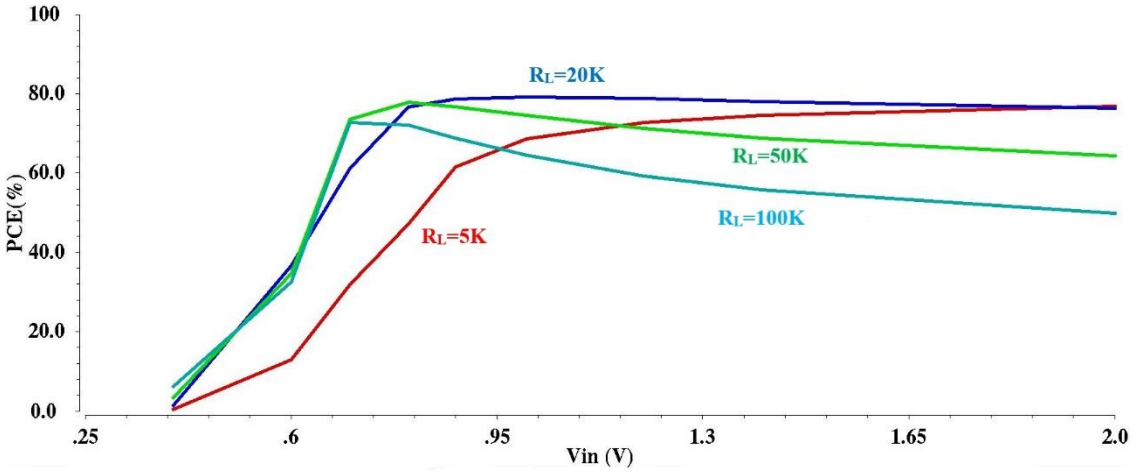

Figure 5.7 Load Resistor dependence on PCE

PCE for higher value of resistors are shifted towards left side (towards low input voltages). This means that the larger PCE can be obtained at low inputs when the load resistor is large. PCE of 78% is obtained at 0.8V input when load resistor is 50KΩ. Also, PCE of 72% is obtained at 0.7V input when load resistor is 100KΩ. This means that communication or wireless power transmission (biomedical application) can be done at such low input with high PCE.

5.3.3 PCE dependence on Transistor sizing

The rectifier transistor ratios affects the performance in PCE which is clearly visible in Figure 5.8

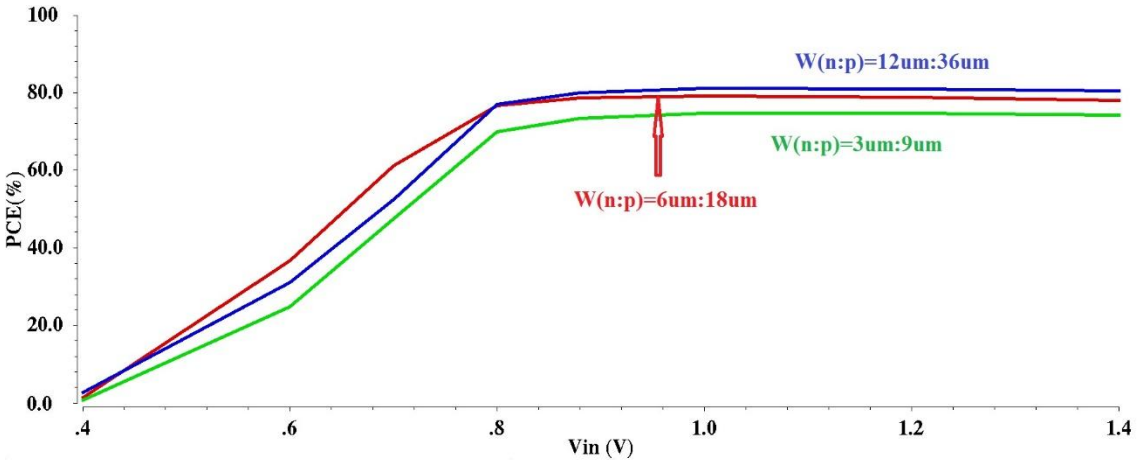

Figure 5.8 PCE as a function of transistor sizing

The transistor width sizes are 6µm (NMOS) and 18µm (PMOS) while length of these transistors are same 0.15µm. The width sizes of transistor are designed to be narrowed (half) and wider (double) while maintaining the width ratio of NMOS and PMOS same i.e. 3 for balanced function of rectifier as can be seen in Figure 5.7.

The reverse leakage current for NMOS transistor is negligible. So, the basic factor is ON resistance of the transistor. From input signal of 0.8V the wider transistor has more PCE than the narrower ones at R_L=20KΩ and it achieves larger peak PCE of 77%. This is because the wider transistor have small ON resistor than the narrower ones at this load. The wider transistor is better at high input voltages as there is no worry for reverse leakage currents in the transistors due to self-biased op-amp. At low input voltage the wider transistor has less PCE than the typical transistors (6um:18um). This is because small ON-resistance of the diodes achieved by the wider transistors under this output loading condition is not much effective for reaching huge PCE than the negligible leakage reverse current achieved by the typical transistors (NMOS).

5.4 Hybrid CMOS rectifier – Other possible topologies

The two other topologies can designed from Hybrid Rectifier

i. For the design of Hybrid rectifier in Figure 5.1, one can use only one op-amp instead of two as one op-amp means less power consumption but power consumption is in nW as seen in Chapter 4. If one of the op-amp is removed from Figure 5.1 then reverse leakage from that NMOS transistor is more resulting in degrading the efficiency.

ii. The other design can be two op-amps with two PMOS transistors rather than NMOS. This design will give less output DC voltage and hence less PCE. The reason is that circuit operation changes when this design is applied. Both PMOS and NMOS in the same node is ON simultaneously resulting in poor performance. For this design to work, change in operating frequency and change in value of capacitance is required.

5.5 Multistage Differential Rectifier

PCE as a function of output DC voltage is obtained for several inputs as can be seen in Figure 5.9. The output voltage form 0.35 to 0.95V is obtained for PCE's greater than 60% at different loading condition.

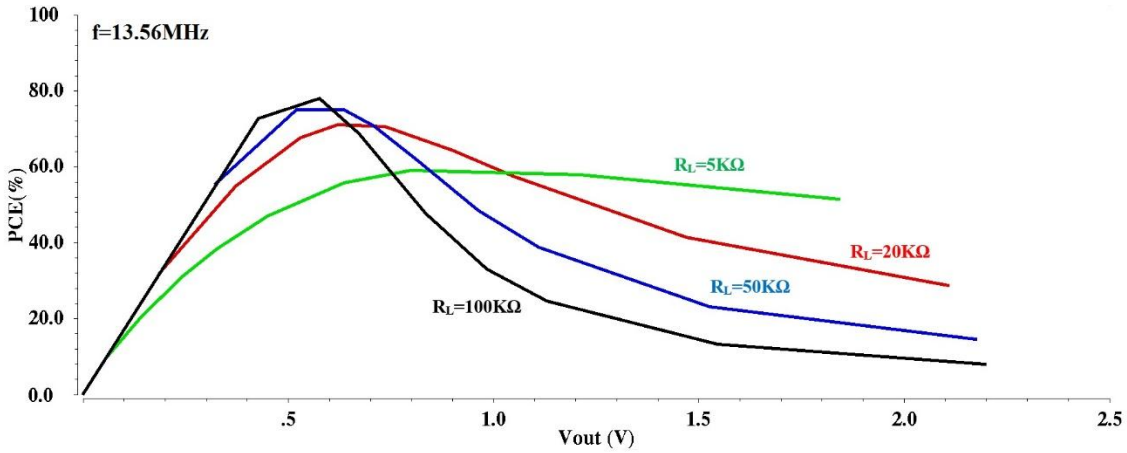

Figure 5.9 PCE as a function of Output DC Voltage (V_{out})

Sometimes higher DC voltage is needed for biomedical implant circuits and digital baseband circuits in RFID at low input voltages for its proper operation while maintaining feasible PCE [11]. For larger output voltage multistage configuration can be used as shown in Figure 5.10

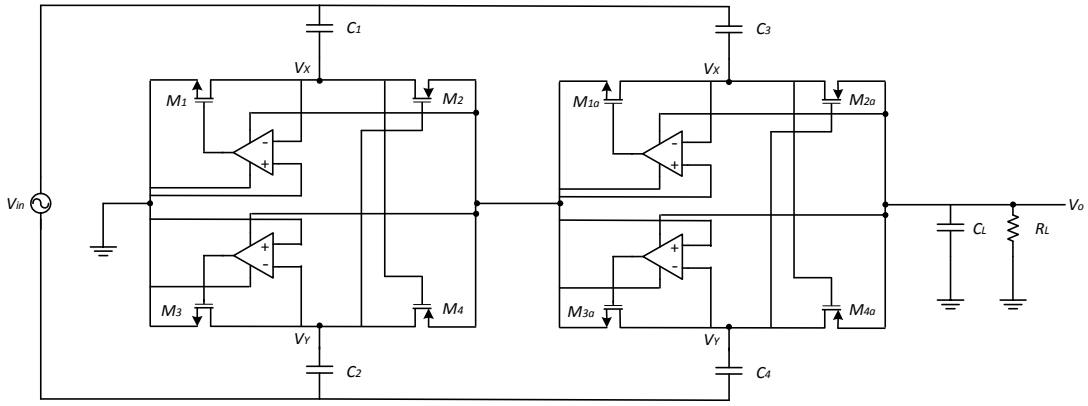

Figure 5.10 Multistage Rectifier

The stages are serially cascaded to each other along the DC path and merged in parallel from the differential input signal. This scheme can be used to obtain larger DC output voltage and is operated to the point where greater PCE can be reached. The first stage output capacitor which is now the inner stage capacitor can be of small value or can be

removed. If the NMOS and PMOS between the two stages are well matched, smaller value of capacitance can minimize the ripple. The two stage rectifier is simulated and the output DC voltage and PCE is plotted to understand its operation. These results are compared with single stage rectifier.

Figure 5.11 shows the output DC voltages of single stage and double stage as function of input voltage. For smaller inputs the output voltages for both the schemes are almost same (double little bit higher) but it increases as the input voltage increases.

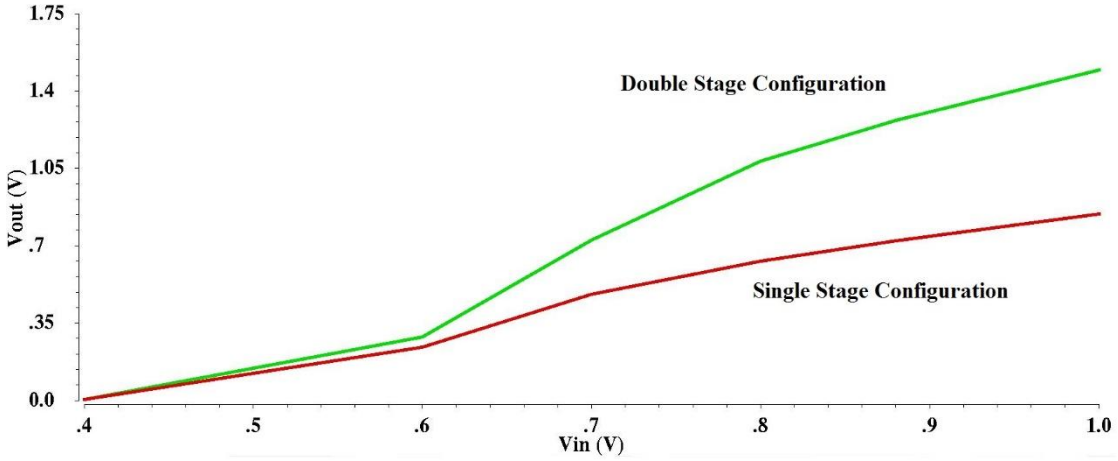

Figure 5.11 Output voltage vs Input voltage (Single and Double Stage compared)

PCE becomes almost same as of single-stage rectifier at low input signal (0.4V) in the multi-stage scheme. It slightly decreases at high input voltages. The stages are merged in parallel to the input signal as mentioned earlier and it supresses the rectifier's input impedance in the multi-stage configuration. This results in the reduction in PCE since adequate RF voltage amplitude larger than the V_{th} of CMOS transistor is necessory for attaining larger PCE. For example, when the input voltage is 1V, sufficient DC voltage of

1.53V is obtained while maintaing 75% of PCE when related to single stage rectifier. The single stage rectifier has 79.12% PCE with 0.85V DC output voltage.

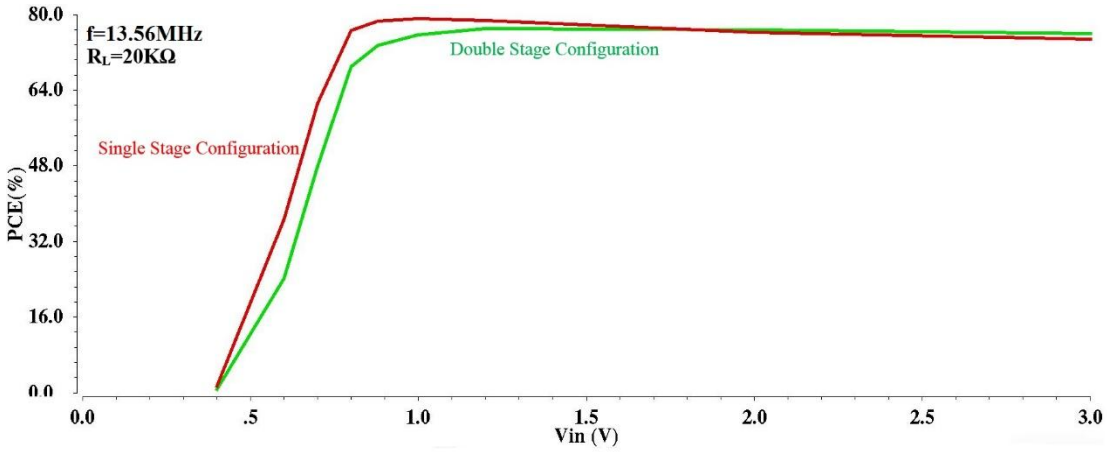

Figure 5.12 PCE vs Input voltage (Single and Double Stage compared)

5.6 Conclusion

A high-efficiency CMOS Hybrid rectifier circuit for HF RFID and biomedical implants applications with an active V_{th} cancellation configuration is proposed. The circuit reduces the V_{th} of CMOS transistors in a forward bias and enhance it in a reverse bias by a cross-coupled circuit scheme. The hybrid rectifier circuit has enormous PCE at lesser input voltage. For example, hybrid rectifier scheme achieves PCE of 79.12% at 13.56 MHz, 0.88V of input amplitude and 20KΩ of output loading, 11.62% more than the CMOS differential rectifier [11]. The multi-stage scheme was assessed as to be effective in order to realize large output DC voltage without reducing PCE. For example, when the input voltage is 1V, enough output DC voltage of 1.5V is obtained while maintaining 76% of PCE when compared to single stage rectifier. The single stage rectifier has 79.12% PCE with 0.85V DC output voltage.

5.7 Comparison with state of art Rectifiers

The comparison of hybrid active rectifiers with the available solutions is summarized in the Table 5.3. The comparison is made for the rectifiers operating at high frequency.

Table 5.3 Comparison of Hybrid Rectifier to works at high frequency in literature

Reference	[11]	[12]	[23]	[1]	[7]	[31]	[43]	This Work
Year	2009	2008	2011	2012	2013	2014	2016	2017
Technology	0.18um	0.25um	0.35um	0.18um	0.13um	0.35um	0.18um	0.15um
Topology	Differential Self-driven rectifier	Voltage doubler using PMOS Floating gate (36 stages)	Threshold Compensated Diode scheme (5 stages)	Gate cross coupled rectifier with bootstrap technique	Reconfigurable Differential CMOS rectifier	Active Rectifier with switched offset and compensated biasing	Self-Biased Cross Coupled rectifier	Differential Hybrid Rectifier
Input Voltage	0.88V	125mV	0.5V	0.8V, 1.8V	125mV	1.5V	57mV	0.88V,1.5V
Operating Frequency	953MHz	906MHz	13.56MHz	10MHz	868MHz	13.56MHz	433MHz	13.56MHz
Output Voltage	0.6V	3V	2.5V	0.3V, 1.2V	2V	1.19V	1V	0.73V,1.32V
Area	NA	0.400 um^2	NA	0.61mm^2	0.2 mm^2	0.186 mm^2	0.017 mm^2	-
PCE	67.5%	60%	37.8%	37%, 71%	60%	81%	65%	79.12%, 78.5%
Output Power	NA	NA	35.8uW	NA	NA	24.8mW	X	25.12uW, 83uW
Load Capacitor and Resistor	C_L=1.13pF R_L=10KΩ	R_L=0.33MΩ	C_L= 80pF R_L= 180kΩ	R_L=2KΩ C_L= 200pF	NA	R_L=500Ω C_L=1.5nF	R_L=50kΩ	C_L=40pF R_L=20KΩ

It can been form Table 5.3 that the passive rectifier solutions such as [11], [12] and [23] can process high frequency input signals which is the typical case of harvesting systems. But they achieve relatively low PCE in the range of 37.8% to 67.5%. The Gate cross coupled rectifier with bootstrap technique [1] achieves low PCE of 37% at 0.8V with 0.3V DC output but achieves relatively low PCE (71%) at high input voltage (1.8V). The

reconfigurable rectifier of [7] showed an improved sensitivity but failed to improve the efficiency (efficiency of 60% was reported) and also they didn't mentioned output loading condition. An active rectifier [31] achieves 81% PCE at 13.56MHz but at high input voltage of 1.5V. The self-biased cross coupled rectifier [43] achieves good sensitivity but has low PCE of 65% when compared to [11] and the proposed design. The proposed integrate-able hybrid rectifier design combines both active and passive to extract maximum PCE of 79.12% at 0.88V when R_L=20KΩ with operating frequency of 13.56MHz. The efficiency increases to 79.12% when R_L increases and remains constant for higher value of loads. So, the differential hybrid rectifier design is built to be used for applications such as biomedical implants and WSNs that are operating in HF band (3-30MHz) for RF signals.

The proposed differential hybrid rectifier is also well suited for low frequency (100 Hz) as op-amp performs better at low frequency. The proposed hybrid rectifier is not fully integrate able as value of load capacitance is set to 1uF. The comparison of hybrid active rectifiers at low frequency (100Hz) with the available solutions is summarized in the Table 5.4.

The design in [24] and [25] gives high efficiency of 90% at very low frequency (100/200Hz) as op-amp works well at low frequency. The Self-Powered Rectifier with Automatic Resetting of Transducer Capacitance [40] is built for higher input voltages (3V) giving maximum efficiency of 91.2% at R_L=100KΩ. When proposed hybrid rectifier is operated at low frequency (100Hz), it gives 88.44% efficiency at 0.88V. So, the hybrid rectifier design can also be used for low power applications that are operating at low frequency. For example, the hybrid rectifier can employ PE energy harvesting at low inputs

(0.88V) giving PCE of 88.44% when compared to its counterpart [40] which gives PCE of 91.2% at higher inputs (3V).

Table 5.4 Comparison of Hybrid Rectifier to works at low frequency in literature

Reference	[24]	[25]	[40]	This Work
Year	2011	2012	2015	2017
Technology	0.35um	0.18um	0.18um	0.15um
Topology	Comparator based active rectifier	Op-amp based active rectifier	Self-Powered Rectifier with Automatic Resetting of Transducer Capacitance	Differential Hybrid Rectifier
Input Voltage	0.5V	2.8V	3V	0.88V
Operating Frequency	100Hz	200Hz	200Hz	100Hz
Output Voltage	0.4V	2.78V	2.9V	0.77V
Area	0.072 mm^2	0.24 mm^2	0.016 mm^2	-
PCE	86%	90%	91.2%	88.44%
Output Power	25uW	81uW	82.1uW	11uW
Load Capacitor and Resistor	R_L=50kΩ C_L=10uF	R_L=95kΩ C_L=1uF	R_L=100kΩ	R_L=50KΩ C_L=1uF

CHAPTER 6

POST LAYOUT SIMULATION

The post layout simulations of the proposed differential hybrid rectifier is done in this last chapter. This chapter outlines the layout of the proposed design and how simulations are affected after layout extraction.

6.1 Layout of Hybrid Rectifier

The layout of differential hybrid rectifier design is shown in Figure 6.1. The layout is carried out in Cadence® with LF 0.15um CMOS technology. The layout of the proposed rectifier covers the area of 0.0023 mm^2. The Layout excludes off chip capacitors and load.

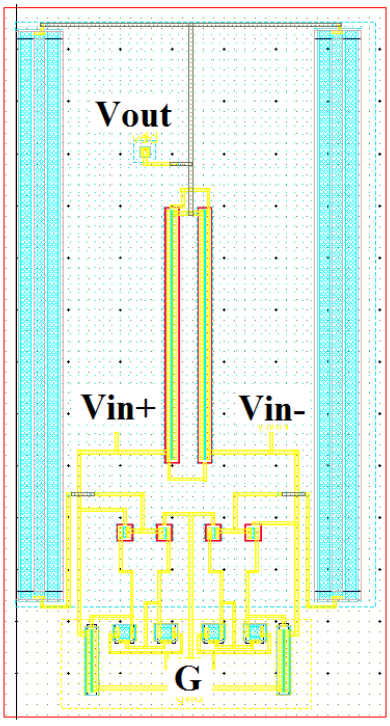

Figure 6.1 Layout of Differenial Hybrid Rectifier

6.2 Post Layout Simulation of Hybrid Rectifier

Post-layout simulation is basically used to confirm the concluded design and confirms all design constraints. Post-layout simulation likewise proves to be useful when relating simulation versus measurements. This is critical to guarantee that the constraints made by pre-layout simulation depends on modeling of the PCB. The designer should alter some of the transistor dimensions and/or the circuit topology if the results of post-layout simulation are not satisfactory, in order to achieve the desired circuit performance taking into account all of the circuit parasitic. An acceptable outcome in post-layout simulation is still no assurance for a totally successful prototype; the real performance of the chip can only be confirmed by testing the fabricated prototype.

6.2.1 PCE dependence on Input Signal and load

The PCE dependence on Input signal of Hybrid CMOS rectifier circuit is post simulated and is compared with schematic only simulations as shown in Figure 6.2.

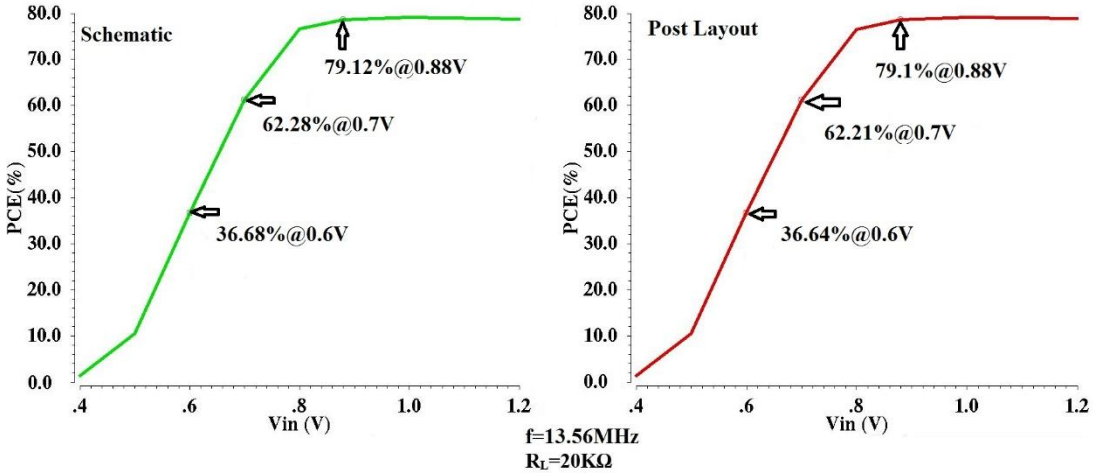

Figure 6.2 PCE as function of V_{in} (Schematic vs Layout)

The off chip capacitors value of 40pF are used for post layout simulation. It can be seen that schematic and post layout simulations are approximately the same. The minor variations in the results are caused due to the parasitic in connections and integrated components. The errors in the proposed circuit will be due to non-ideality in the circuit and it will be analyzed once the chip is fabricated. The post layout simulations results are satisfactory as small errors occurred when the two simulations are compared. The summary of Figure 6.2 can be written as shown in Table 6.1.

Table 6.1 Post PCE and Output Voltage when R_L=20KΩ

Vin=0.6V	Different Hybrid	Differential Hybrid - Extracted
Vout (V)	0.242	0.241
PCE (%)	36.68	36.64
Vin=0.7V		
Vout (V)	0.481	0.48
PCE (%)	62.28	62.21
Vin=0.88V		
Vout (V)	0.73	0.728
PCE (%)	79.12	79.1

The PCE dependence on the output loading condition of Hybrid CMOS rectifier circuit is post simulated and is compared with schematic only simulations as shown in Figure 6.2.

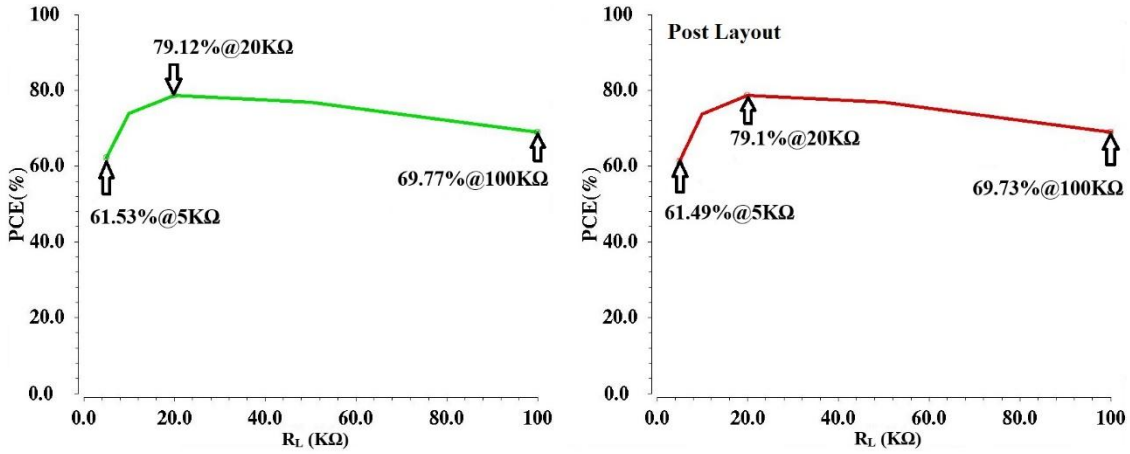

Figure 6.3 PCE as a function of R_L

The minor variations in the results are caused due to the parasitic in connections and integrated components. The post layout simulations results are also satisfactory as small errors occurred when the two simulations are compared. The summary is shown in Table 6.2.

Table 6.2 Post PCE and Output Voltage when V_{in}=0.88V

R_L =5K	Hybrid - (13.56MHz)	Hybrid - Extracted (13.56MHz)
Vout (V)	0.547	0.547
PCE (%)	61.53	61.49
R_L =20K		
Vout (V)	0.721	0.721
PCE (%)	79.12	79.1
R_L =100K		
Vout	0.793	0.792
PCE (%)	69.77	69.73

CHAPTER 7

CONCLUSION AND FUTURE WORK

The conclusion and inferences of the thesis are summarized in this chapter. This chapter outlines the considered problem, the proposed solution and analysis of the results. At the end, a discussion on the prospects of extending this work in future is demonstrated.

7.1 Conclusion

The purpose of this research is to design a Differential Hybrid CMOS Rectifier with lower power consumption than the available solutions while keeping the input sensitivity of the rectifier design. This idea was to combine passive and active rectifier structures to form a hybrid rectifier to get maximum PCE as that of active rectifiers alone. The first objective was the reduction of power consumption for the hybrid rectifier design which is achieved by making the forward drop to zero and reverse leakage current negligible by using differential rectifier technique with op-amp and then optimizing to get the required results. The next step was keeping the input sensitivity comparable while going higher with the PCE.

The hybrid rectifier circuit has enormous PCE at lesser input voltage. For example, hybrid rectifier scheme achieves PCE of 79.12% at 13.56 MHz, 0.88V of input amplitude and 20KΩ of output loading, 11.62% more than the CMOS differential rectifier [11].

The multi-stage scheme was assessed as to be effective in order to realize large output DC voltage without reducing PCE. For example, when the input voltage is 1V, enough output

DC voltage of 1.5V is obtained while maintaing 76% of PCE when compared to single stage rectifier. The single stage rectifier has 79.12% PCE with 0.85V DC output voltage. While in the designs of [24] and [25] they achive high efficiency without doubling the voltage and also they are not integrateable. When compared to design in [31], efficiency is same as of proposed hybrid rectifier design but at high amplitudes.

7.2 Future Work

This work can be continued by fabricating the design to make the chip of this hybrid rectifier circuit. After fabrication, the testing can be performed and the results will be analyzed. The proposed circuit is for Differential signals, it can be converted into single ended by PCB balun. The op-amp can be designed for high unity gain frequency but one has to be careful for not reducing the PCE of the design. The output DC voltage from the 1^{st} or 2^{nd} stage of the rectifier can be utilized to supply the op-amp. The input of the op-amp can be another energy source say PE source at low frequency and it is amplified by this op-amp. This scheme will be useful when there are two energy source available.

References

[1] S. Hashemi, M. Sawan, and Y. Savaria, "A High-Efficiency Low- Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices," *IEEE Transaction on Biomedical Circuits and Systems*, vol. 6, no. 4, pp. 326-335, Aug. 2012.

[2] Y. Tan, and S. Panda, "Optimized Wind Energy Harvesting System Using Resistance Emulator and Active Rectifier for Wireless Sensor Nodes," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 38-50, Jan. 2011.

[3] Prusayon Nintanavongsa, Ufuk Muncuk, David Richard Lewis, and Kaushik Roy Chowdhury, "Design Optimization and Implementation for RF Energy Harvesting Circuits", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1,pp. 24-33, March 2012

[4] M. Kroener, "Energy Harvesting Technologies: Energy Sources, Generators and Management for Wireless Autonomous Applications" *9th International Conference on Systems, Signals and Devices*, 2012

[5] Prusayon Nintanavongsa, Ufuk Muncuk, David Richard Lewis, and Kaushik Roy Chowdhury, "Design Optimization and Implementation for RF Energy Harvesting Circuits", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, March 2012

[6] Yen Kheng Tan, and Sanjib Kumar Panda, "Optimized Wind Energy Harvesting System Using Resistance Emulator and Active Rectifier for Wireless Sensor Nodes" *IEEE Transactions on Power Electronics*, vol. 26, no. 1, January 2011

[7] S. Scorcioni, L. Larcher, and A. Bertacchini, "A Reconfigurable Differential CMOS RF Energy Scavenger With 60 % Peak Efficiency and -21 dBm Sensitivity" *IEEE Microwave and Wireless Components Letters*, vol 23, no. 3, March 2013

[8] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[9] Jungmoon Kim, Jihwan Kim, Minseob Sim, Soowon Kim, and Chulwoo Kim, "A Single-Input Four-Output (SIFO) AC–DC Rectifying System for Vibration Energy Harvesting", *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2629 – 2633, June 2014.

[10] Xinping Cao, Wen-Jen Chiang, Ya-Chin King, and Yi-Kuen Lee, "Electromagnetic Energy Harvesting Circuit With Feedforward and Feedback DC–DC PWM Boost Converter for Vibration Power Generator System" *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 679 – 685, March 2007.

[11] K. Kotani, A. Sasaki, and T. Ito, "High-efficiency differential-drive CMOS rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, 44(11), pp.3011-3018, Nov. 2009.

[12] T. Le, K. Mayaram, and T. Fiez, "Efficient far-field radio frequency energy harvesting for passively powered sensor networks," *IEEE J. Solid-State Circuits*, 43(5), pp.1287-1302, May 2008.

[13] S. Oh and D. D. Wentzloff, "A -32dBm Sensitivity RF Power Harvester in 130nm CMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 483-486, 2012.

[14] H. Nakamotoa, D. Yamazakia, T. Yamamotoa, H. Kurataa, S. Yamadaa, K. Mukaidaa, T. Ninomiyaa, T. Ohkawaa, S. Masuia, and K. Gotoha, "A passive UHF RFID tag LSI with 36.6% efficiency CMOS-only rectifier and current-mode demodulator in 0.35um FERAM technology," *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 310–311, Feb. 2006.

[15] T. Umeda, H.Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor network tags with 10-m distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[16] T. Le, J. Han, A. von Jouanne, K. Mayaram, and T. S. Fiez, "Piezoelectric power generation interface circuits," *Proc. IEEE Custom Integrated Circuit Conf. (CICC)*, pp. 489–492, Sept. 2003.

[17] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-um technology," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 101-110, Jan. 2007.

[18] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuit with self-Vth-cancellation and power regulation functions for UHF RFIDs," Proc. IEEE ASSCC, pp. 119-122, Nov. 2007.

[19] K. Kotani and T. Ito, “Self-Vth-cancellation high-efficiency CMOS rectifier circuit for UHF RFIDs,” IEICE Trans. Electron., vol. E92-C, no. 1, pp. 153-160, Jan. 2009.

[20] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, F. De Flaviis, “Power harvester design for passive UHF RFID tag using a voltage boosting technique,” *IEEE Trans. Microw. Theory Tech.*, 55(6), pp.1089-1097, June 2007.

[21] S. Mandal and R. Sarpeshkar, "Low-power CMOS rectifier design for RFID applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, 54(6), pp.1177-1188, June 2007.

[22] A. Sasaki, K. Kotani, and T. Ito, “Differential-drive CMOS rectifier for UHF RFIDs with 66% PCE at -12dBm input,” in *Proc. IEEE ASSCC*, pp. 105–108, Nov. 2008.

[23] H. Xu, and M. Ortmanns, “A Temperature and Process Compensated Ultralow Voltage Rectifier in Standard Threshold CMOS for Energy-Harvesting Applications” *IEEE Transactions on Circuits and Systems -II: Express Briefs*, vol. 58, no. 12, pp. 812 – 816, December 2011.

[24] C. Peters, J. Handwerker, D. Maurath, and Y. Manoli, “A Sub-500 mV Highly Efficient Active Rectifier for Energy Harvesting Applications”, *IEEE Transactions on Circuits and Systems - I*, vol. 58, no. 7,pp. 1542 – 1550, July 2011.

[25] Y. Sun, N. Hieu, C.-J. Jeong, and S.-G. Lee, “An Integrated High Performance Active Rectifier for Piezoelectric Vibration Energy Harvesting Systems”, *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 623 – 627, February 2012.

[26] R. Glidden, C. Bockorick, S. Cooper, C. Diorio, D. Dressler, V. Gutnik, C. Hagen, D. Hara, T. Hass, T. Humes, J. Hyde, R. Oliver, O. Onen, A. Pesavento, K. Sundstrom, and M. Thomas, "Design of ultra-low-cost UHF RFID tags for supply chain applications," *IEEE Commun. Mag.*, vol. 42, no. 8, pp. 140–151, Aug. 2004.

[27] J.-D. Tseng, W.-D. Wang, and R.-J. Ko, "An UHF band RFID vehicle management system," in *Proc. 2007 IEEE Int. Workshop on Anticounterfeiting, Security, Identification*, Apr. 2007, pp. 390–393.

[28] S. Chumkamon, P. Tuvaphanthaphiphat, and P. Keeratiwintakorn, "A blind navigation system using RFID for indoor environments," in *Proc. ECTI-CON 2008*, May 2008, vol. 2, pp. 765–768.

[29] Truong Thi Kim Nga, Hyung-Gu Park, and Kang-Yoon Lee, "A High Efficiency Active Rectifier for 6.78MHz Wireless Power Transfer Receiver with Bootstrapping Technique and All Digital Delay-Locked Loop," *IEIE Transactions on Smart Processing and Computing*, vol. 3, no. 6, December 2014.

[30] Jan Kracek; Milan Švanda; Milos Mazanek; Jan Machac, "Implantable Semi-Active UHF RFID Tag With Inductive Wireless Power Transfer," *IEEE Antennas and Wireless Propagation Letters*, vol. 15, pp. 1657 - 1660, January 2016.

[31] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS Active Rectifir With Switched-Offet and Compensated Biasing for Biomedical Wireless Power Transfer Systems," IEEE Trans. on Biomedical Circuits and Systems, vol. 8, Issue. 3, pp. 334-344, Jun 2014

[32] Prusayon Nintanavongsa, Ufuk Muncuk, David Richard Lewis, and Kaushik Roy Chowdhury, "Design Optimization and Implementation for RF Energy Harvesting Circuits", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 2, no. 1, March 2012

[33] Andre Mansano, Sumit Bagga, and Wouter Serdijn, "A High Efficiency Orthogonally Switching Passive Charge Pump Rectifier for Energy Harvesters" *IEEE Transactions on Circuits and Systems – I*, vol. 60, no. 7, July 2013.

[34] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of UHF micro-power CMOS rectifiers for micro-sensor and RFID applications," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 1, pp. 153–166, Jan. 2007.

[35] A. Ashry, K. Sharaf, and M. Ibrahim, "A simple and accurate model for RFID rectifier," *IEEE Syst. J.*, vol. 2, no. 4, pp. 520–524, Dec. 2008.

[36] J. Crols and M. Steyaert, "Switched-Opamp: An Approach to Realize Full CMOS Switch-Capacitor Circuits at Very Low Power Supply Voltage," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 936-942, Aug. 1994.

[37] X. D. Do, Y. H. Ko, H. H. Nguyen, H. B. Le, and S. G. Lee, "An efficient parallel SSHI rectifier for piezoelectric energy scavenging systems," in Proc. IEEE Int. Conf. Adv. Commun. Technol., 2011, pp. 1394–1397.

[38] S. Roundy, P. Wright, and J. Rabaey, Energy Scavenging for Wireless Sensor Network with Special Focus on Vibrations. Boston, MA, USA: Kluwer Academic, 2003.

[39] Adel S. Sedra, Kenneth C. Smith, *Microelectronic Circuits*, 6th ed., Oxford University Press, 2009

[40] Xuan-Dien Do, Huy-Hieu Nguyen, Seok-Kyun Han, Dong Sam Ha, and Sang-Gug Lee, "A Self-Powered High-Efficiency Rectifier With Automatic Resetting of Transducer Capacitance in Piezoelectric Energy Harvesting Systems", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 3, March 2015.

[41] D.M. Monticelli, "A quad CMOS single-supply op amp with rail-to-rail output swing", *IEEE Journal of Solid-State Circuits*, vol. 21, no. 6, December 1986.

[42] E. Dallage et al., "Active self supplied AC-DC converter for piezoelectric energy scavenging systems with supply independent bias," in Proc. IEEE Int. Symp. Circuit Syst. Conf., May 2008, pp. 1448–1451.

[43] Mahmoud H. Ouda, Waleed Khalil, Khaled N. Salama, "Self-Biased Differential Rectifier with Enhanced Dynamic Range for Wireless Powering", *IEEE Transactions on Circuits and Systems - II*, vol. PP, no. 99, December 1986.

LIST OF PUBLICATIONS

[C1] Umais Tayyab, Hamza Shahid, Hussain Alzaher, "A self-biased active precision rectifier for energy harvesting systems", presented in 14th International Multi-Conference on Systems, Signals & Devices (SSD), Marrakech, Morocco, March 2017.

[C2] Hamza Shahid, Umais Tayyab, Hussain Alzaher, "A CMOS Timer Circuit with Pulse Width Modulation for Sub-hertz Monitoring Applications", presented in 14th International Multi-Conference on Systems, Signals & Devices (SSD), Marrakech, Morocco, March 2017.

[C3] Muhammad Taha Ali, Ali Anwar, Umais Tayyab, Yasir Iqbal, Tauseef Tauqeer, Usman Nasir, "Design of high efficiency wireless power transmission system at low resonant frequency", 16th International Power Electronics and Motion Control Conference and Exposition, Antalya, Turkey 21 -24, Sept 2014

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